

1. Operational Amplifier

IC (Integrated Circuit):- IC is a miniature (small in size) low cost electronic circuit consisting of active and passive components that are irreparably join together on a single crystal chip of Silicon. Most of the components used in ICs are not similar to conventional components in appearance although they perform similar electrical functions.

Advantages of Integrated Circuits:-

1. Miniaturization (small in size) hence
2. increased equipment density,
2. Cost reduction due to batch processing.
3. Increase system reliability due to elimination of solder joints
4. Improved functional performance
5. Matched device
6. Increased operating speed (due to decrease of parasitic capacitive effect)
7. Reduction in power consumption.

Disadvantages of Integrated Circuits:-

1. Inductors & Transformers cannot be fabricated on IC
2. The large value of capacitor cannot be fabricated on IC.

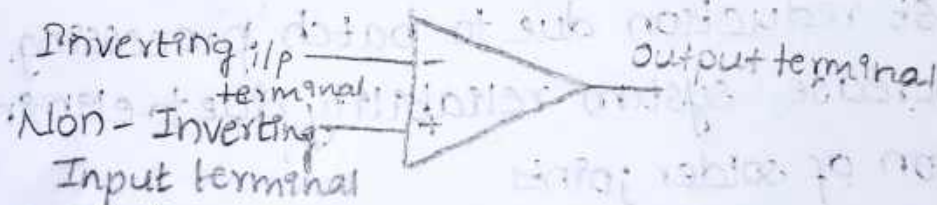
3. It can handle only limited amount of power (upto 10W)

Applications

- * In all Communication fields (mobile communication, Satellite, Radar & Wireless Communications).
- * Home Appliances (Radio, TV, Refrigerator, AC, Washing Machine, Oven)
- * In Medical fields
- * Instrumentation and control etc.

Operational Amplifier

Symbol of Op-Amp:



* It has two input terminals and one Output terminal.

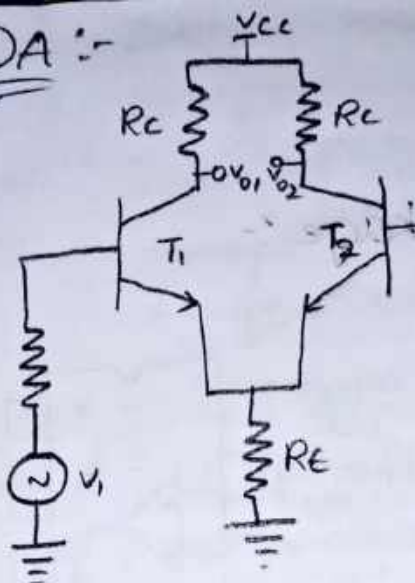
* The terminal with -ve sign is called Inverting Input terminal.

* The terminal with +ve sign is called Non-Inverting Input terminal.

Internal structure of Op-Amp (Block diagram)



DA :-



Types of DA :-

- i) Dual i/p: balanced DA
- ii) Dual i/p: unbalanced Differential amplifier
- iii) Single input balanced differential amp.
- iv) Single input unbalanced differential amplifier.

Operational Amplifier :-

Operational Amplifier is popularly known as Op-Amp is a very high gain direct coupled amplifier with high input impedance and low output impedance.

In Analog computers it is used to perform several mathematical operations like Summing, multiplication by a constant, Integration, Differentiation, log and anti-log operations to amplify the signals, to generate the signal like sine wave, square wave, triangular wave and sawtooth wave and convert the signal from digital to Analog (DAC) and Analog to digital (ADC) etc.. So, the IC 741 is called Operational Amplifier.

Packages :-

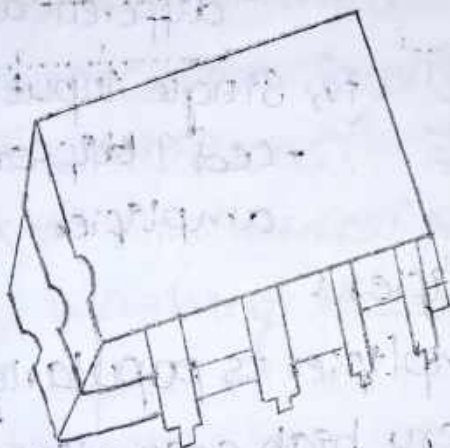
The three popular packages are

- i) Dual in Plastic Package (DIP)

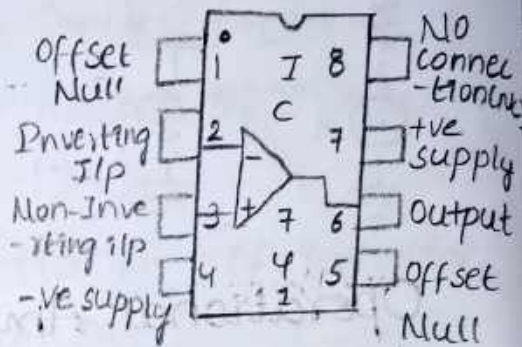
i) Metal Can Package

ii) Flat package

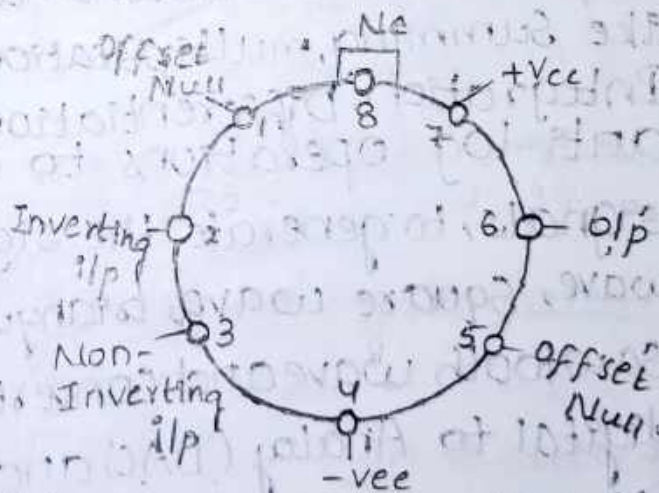
3. Dual-in-Plastic Package :-



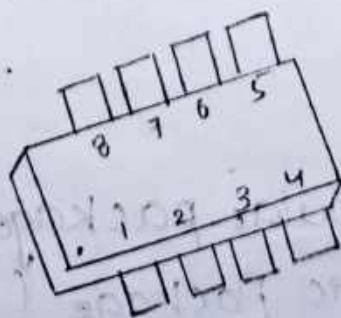
DIP Package



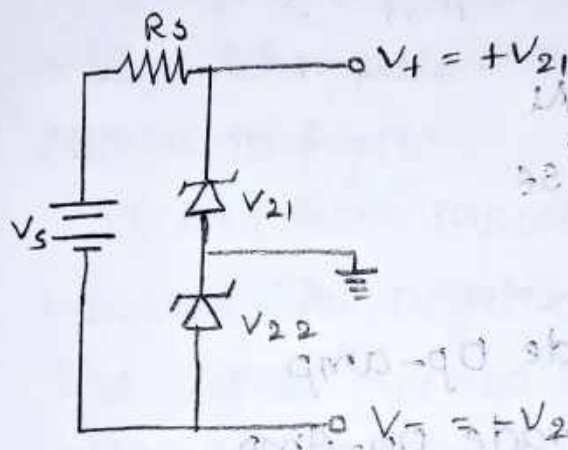
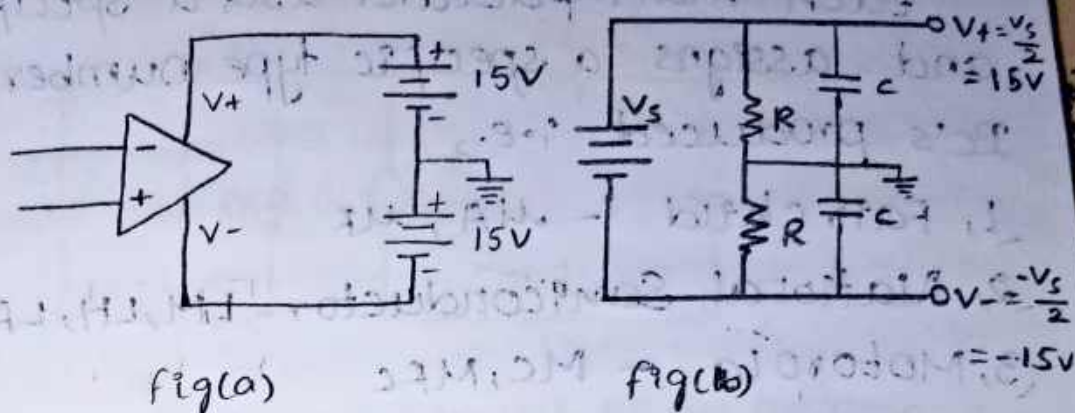
i) Metal Can Package



ii) Flat Package :-



Power supply connections for 741 IC



Fig(c):

In fig(a) the power supply to 741 IC by using dual regulated power supply

If fig (b) & (c) the power supply connections of 741 IC by using single mode power supply

Temperature Ranges:-

All integrated circuits manufactures fall into one of the 3 basic temperature range.

- 1, Military Temperature Range $\rightarrow -55^\circ$ to $+125^\circ$
- 2, Industrial Temp. Range $\rightarrow -20^\circ$ to $+85^\circ$
- 3, Commercial Temp. Range $\rightarrow 0^\circ$ to $+70^\circ$

Manufacturer designation for linear ICs

Each manufacturer uses a specific code and assigns a specific type number to the IC's produced i.e.,

- 1, Fairchild - $\mu A, \mu F$
- 2, National Semiconductor - LM, LH, LF, TBA.
- 3, Motorola - MC, MFC
- 4, RCA - CA, CD
- 5, Texas Instrument - SN
- 6, Signetic - N/s, NE/se
- 7, Burr Brown - BB

741 $\rightarrow$ Military grade Op-amp

741C $\rightarrow$ Commercial grade Op-Amp

741A $\rightarrow$ Improved version of 741

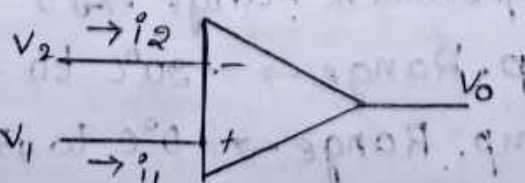
741E $\rightarrow$ Improved version of 741C

741S $\rightarrow$ Military grade Op-amp with higher slew rate

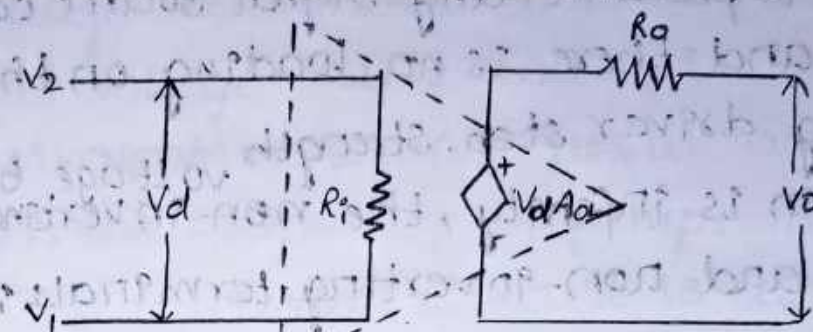
741SC $\rightarrow$ Commercial grade Op-amp with higher slew rate

$$\text{Slew Rate} = \frac{\Delta V_o}{\Delta t}$$

Ideal Op-amp



fig(a):- Ideal Op-amp



Fig(b): Equivalent circuit of an op-amp

The schematic symbol of op-amp is shown in fig(b).

It has two input terminals and one output terminal. The negative and positive symbols at the input referred to inverting and non-inverting input terminals respectively, i.e.,

If $V_1 = 0$, the output voltage V_o is 180° out of phase with input signal V_2 .

When $V_2 = 0$ the output V_o will be in phase with the input signal applied at V_1 .

Ideal Op-amp characteristics:

1. Open loop voltage gain $A_{OL} = \infty$
2. Input Impedance $R_i = \infty$
3. Output Impedance $R_o = 0$
4. Bandwidth $BW = \infty$
5. 0 (zero) offset voltage $V_o = 0$ ($V_{offset} = 0$)
when $V_1 = V_2 = 0$
6. An Ideal Op-amp draws low current at both the input terminals i.e., $i_1 = i_2 = 0$

because of infinite input impedance. Because of input impedance, any signal source can drive it and there is no loading on the preceding driver stage. Since gain is infinity, the ~~non-inverting~~ inverting and non-inverting terminals, i.e., differential voltage $V_d = V_1 - V_2$ i.e., essentially zero for a finite output voltage.

The output voltage V_o is independent of the current drawn from the output as $R_o = 0$. Thus the output can drive an infinite number of other devices.

- 7) $i_1 = 0$ or $i_2 = 0$
- 8) Slew Rate (S.R) $= \frac{\Delta V_o}{\Delta t} = \infty$ ($t = \text{time}$)
- 9) CMRR $= \frac{A_d}{A_c} = \infty$ 11) SVRR $= 0$
- 10) Thermal drift $= \Delta A = \frac{\Delta V_o}{\Delta T}$ ($T = \text{Temp}$)

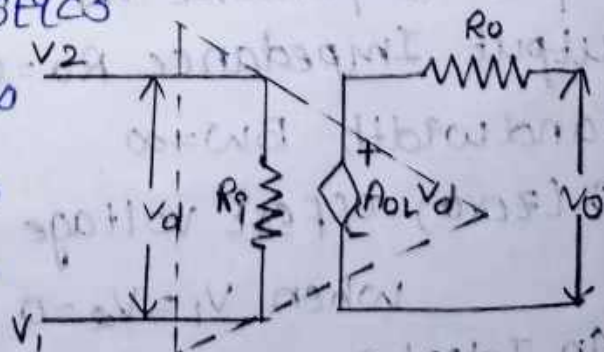
Practical Op-amp Characteristics:

The practical Op-amp that can be made to approximate the some of the ideal characteristics

i) $A_{OL} \neq \infty$

ii) $R_i \neq \infty$

iii) $R_o \neq 0$



It can be seen that op-amp voltage control voltage source ($A_{OL}V_d$) i.e. equivalent therms voltage source and R_o is thevenins equivalent resistance i.e. we are calculating from the output of op-amp.

The equivalent circuit is useful in analysing the basic operating principles of an op-amp.

$$\text{The output voltage } V_o = A_{OL}V_d$$
$$= A_{OL}(V_1 - V_2)$$

The equation shows that the op-amp amplifies the differences between two input voltages.

- * An Ideal Op-amp draws low current from the source and its response is also independent of temperature.
- * However, in real (practical) op-amp does not work in this way it takes some current from the source into the op-amp input terminals and also the two inputs (V_1 & V_2) respond differently to current & voltages due to mismatch in the transistors.
- * A practical op-amp also shifts its operation with temperature.

Non-Ideal (practical) characteristics of an op-amp

1. DC-characteristics

- a) Input bias Current
- b) Input Offset Current
- c) Input Offset Voltage
- d) Total Output offset voltage
- e) Thermal drift

2) AC Characteristics

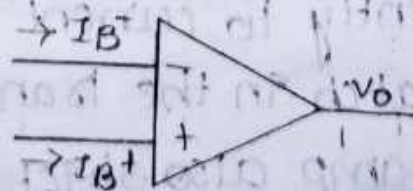
- a) Frequency Response
- b) Stability of an op-amp
- c) Frequency Compensation
- d) Slew Rate

DC Characteristics

Input Bias Current

The op-amp input is a differential amplifier which may be made of BJT or FET.

Practically Input terminals do conduct a small value of DC current to bias the input transistor. The base current entering into the inverting and non-inverting as shown in figure as



Input Bias Current

Even though both the transistors are identical I_B^+ & I_B^- are not equal due to the internal imbalance.

$$I_B = \frac{I_B^- + I_B^+}{2} = \frac{2\mu A + 2\mu A}{2} = 2\mu A$$

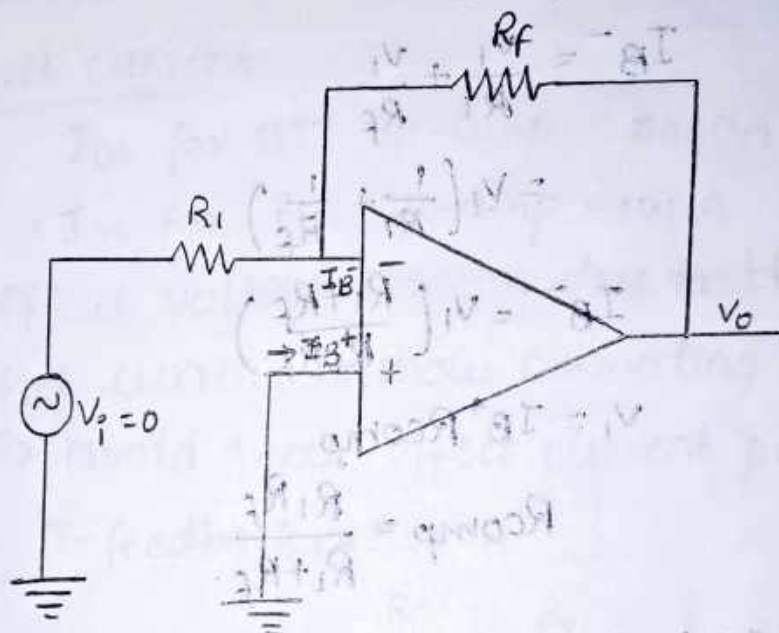
$$V_o = I_B R_f$$

$$I_f = 1\mu A$$

$$I_B = 500\mu A$$

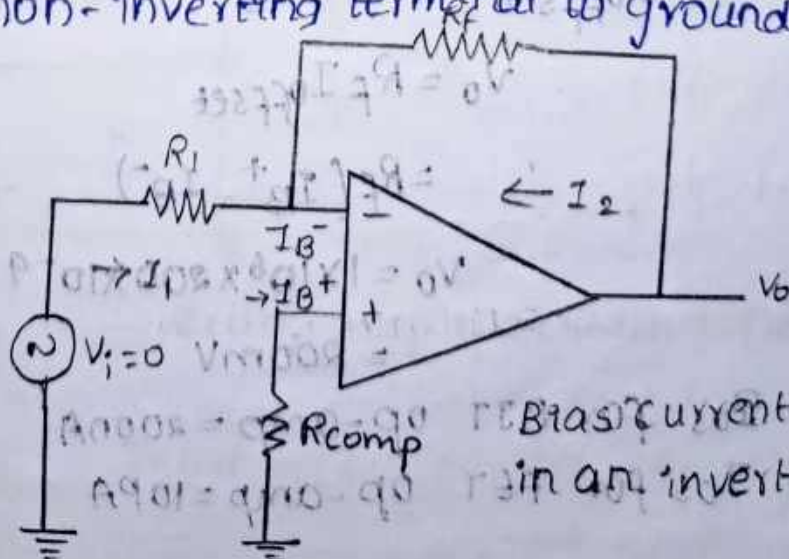
$$V_o = 500 \times 10^{-9} \times 1 \times 10^6$$

$$= 500 \times 10^{-3} \Rightarrow 500\text{mV}$$



Inverting amplifier with bias currents

The output is driven to 500mV with 0 input because of bias currents. The output 500mV is the offset voltage we can compensate by using R_{comp} resistor connected between the non-inverting terminal to ground.



Bias current compensation in an inverting amplifier

$$I_B = I_1 + I_2$$

$$= \frac{V_1}{R_1} + \frac{V_2}{R_f}$$

$$V_d = V_1 - V_2$$

$$V_d = 0 \rightarrow \text{Ideal op-amp}$$

$$0 \times 0 = V_1 - V_2 = 0$$

$$V_1 = V_2$$

$$I_B^- = \frac{V_1}{R_1} + \frac{V_1}{R_f}$$

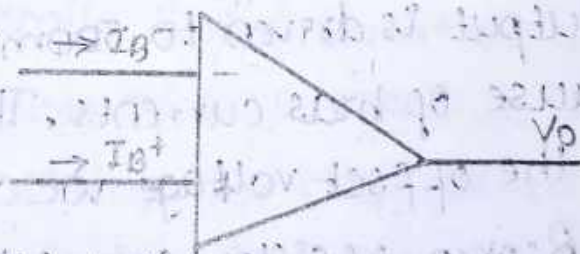
$$= V_1 \left(\frac{1}{R_1} + \frac{1}{R_f} \right)$$

$$I_B^- = V_1 \left(\frac{R_1 + R_f}{R_1 R_f} \right)$$

$$V_1 = I_B^+ R_{comp}$$

$$R_{comp} = \frac{R_1 R_f}{R_1 + R_f}$$

Input offset current:-



$$I_{offset} = I_{B^+} - I_{B^-}$$

$$V_o = R_f I_{offset}$$

$$= R_f (I_{B^+} - I_{B^-})$$

$$V_o = 1 \times 10^6 \times 200 \times 10^{-9}$$

$$= 200 \text{ mV}$$

I_{os} for BJT op-amp = 200 nA

I_{os} for FET op-amp = 10 pA

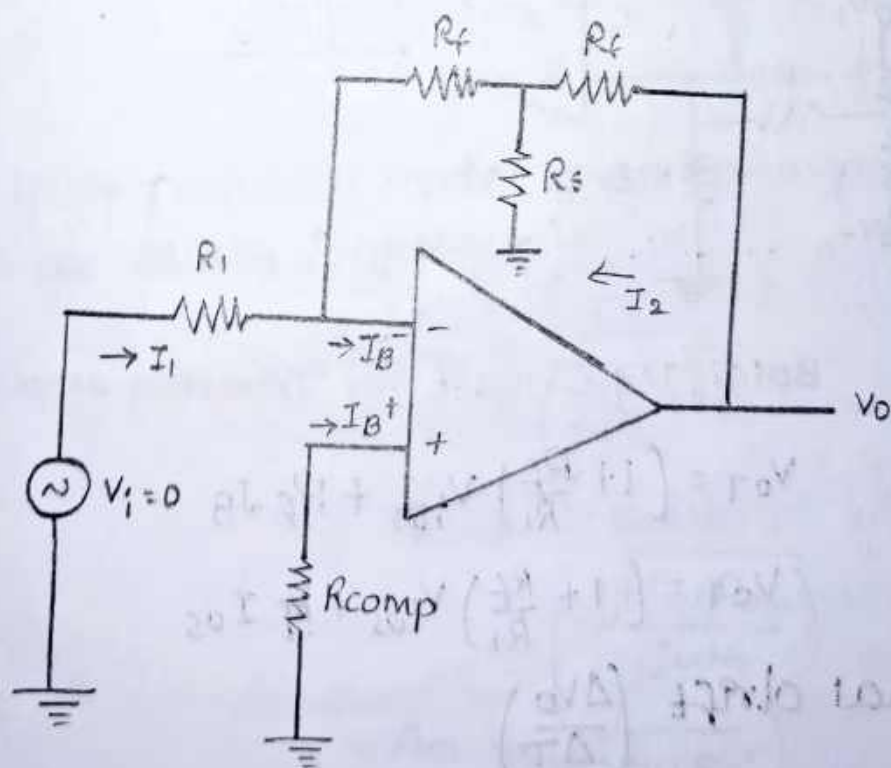
Input offset current, bias current compensation will work if both currents I_{B^+} and I_{B^-} are equal. Since the input transistors cannot be made identical there will always be some difference between I_{B^+} & I_{B^-} . This difference is called offset current.

I_{os} for BJT op-amp = 200 nA

I_{os} for FET op-amp = 10 pA

Offset voltage existing due to the input offset current without connecting any i/p voltage

To avoid input offset current problem we use T-feedback network

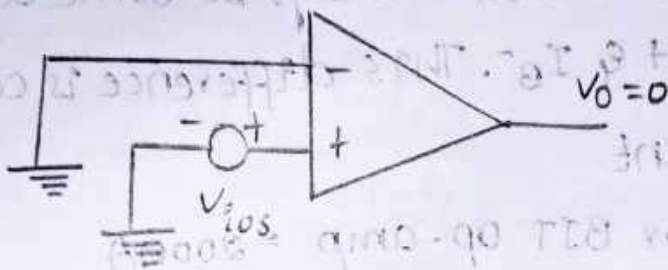


Inverting amplifier with T-feedback n/w

Input offset current compensation ckt

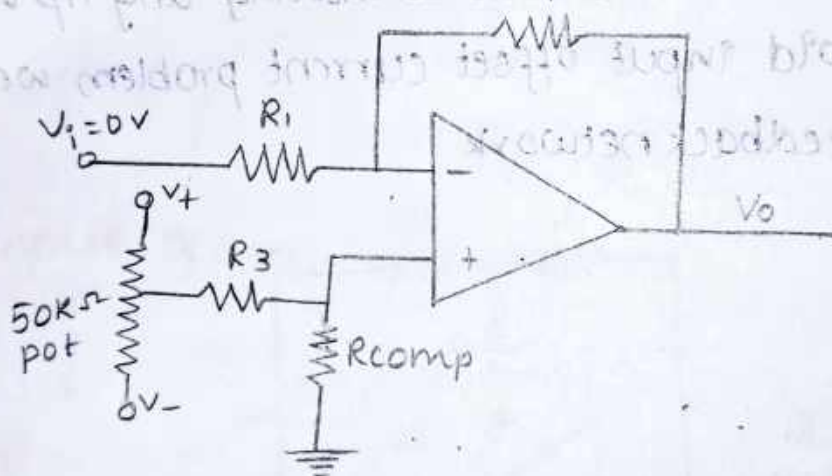
Input offset voltage

This is the voltage required to apply at the input for making output voltage as 0 volts as shown in figure



Op-amp showing input offset voltage

Total output offset voltage:-



Balancing circuit for Inverting amplifier

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{los} + R_f I_B$$

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{los} + R_f I_{os}$$

Thermal drift $\left(\frac{\Delta V_o}{\Delta T}\right)$

Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25°C may not remain same when the temp raises to 25°C . This is called drift.

Offset current drift is expressed in $nA/^\circ C$.

Offset voltage drift is expressed in $mV/^\circ C$.

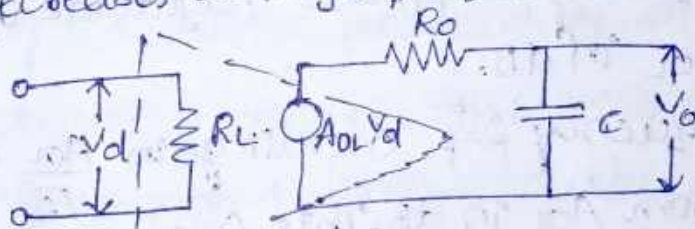
These indicate that change in offset voltage for each $^\circ C$ (change in temp).

To minimize thermal drift

- 1) Careful PCB layout must be used to keep Op-amp away from source.
- 2) Forced air cooling may be used to stabilize the ambient temperature.

AC Characteristics:-

- 1) Frequency Response:- Ideally an op-amp should have infinite bandwidth. The practical op-amp however decreases at high frequencies.



High frequency model of an op-amp with single carrier frequency.

$$V_o = A_{ol} V_d \times \frac{\left(\frac{1}{j\omega C}\right)}{\left(\frac{1}{j\omega C}\right) + R_o}$$

$$V_o = A_{ol} V_d \cdot \frac{\left(\frac{1}{j\omega C}\right)}{\left(\frac{1 + j\omega R_o C}{j\omega C}\right)}$$
$$= A_{ol} V_d \left(\frac{1}{j 2\pi f R_o C} \right)$$

$$= A_{ol} V_d \frac{1}{\left[1 + j\left(f/f_1\right)\right]}$$

where $f_1 = \frac{1}{2\pi R_{OC}}$; f_1 = corner frequency

$$|V_o| = \frac{A_{OL} V_d}{\sqrt{1 + (f/f_1)^2}}$$

$$\frac{V_o}{V_d} = \frac{A_{OL}}{\sqrt{1 + (f/f_1)^2}}$$

$$A = \frac{V_o}{V_i} = \frac{A_{OL}}{\sqrt{1 + (f/f_1)^2}} \quad \phi = \tan^{-1}(f/f_1)$$

for freq (1) $f \ll f_1 \Rightarrow |A| \approx A_{OL}$ $\phi = \tan^{-1}(0) = 0$

(2) $f = f_1 \Rightarrow |A| \approx A_{OL}/\sqrt{2}$ $\phi = \tan^{-1}(1) = 45^\circ$

(3) $f \gg f_1 \Rightarrow |A| \downarrow$

$\Rightarrow$ For frequency $f \ll f_1$, the magnitude of gain is $20 \log A_{OL}$ in dB.

$\Rightarrow$ For frequency $f = f_1$ overall gain $\frac{A_{OL}}{\sqrt{2}}$ i.e., 3dB down from A_{OL} in dB. This frequency f_1 is called corner frequency.

$\Rightarrow$ For frequency $f \gg f_1$ the gain $\downarrow$ at rate of -20dB

$\Rightarrow$ Gain with $A = \frac{A_{OL}}{(1 + j\frac{f}{f_1})(1 + j\frac{f}{f_2})(1 + j\frac{f}{f_3})}$

2) Stability of an op-amp.

Op-amps are rarely ^{used} in open-loop configuration because of its high gain ($A_{OL} = \infty$) for an ideal op-amp.

To achieve the stability of an op-amp

here we connect the op-amp in feedback mode
In this we connect the resistor as of a feedback component

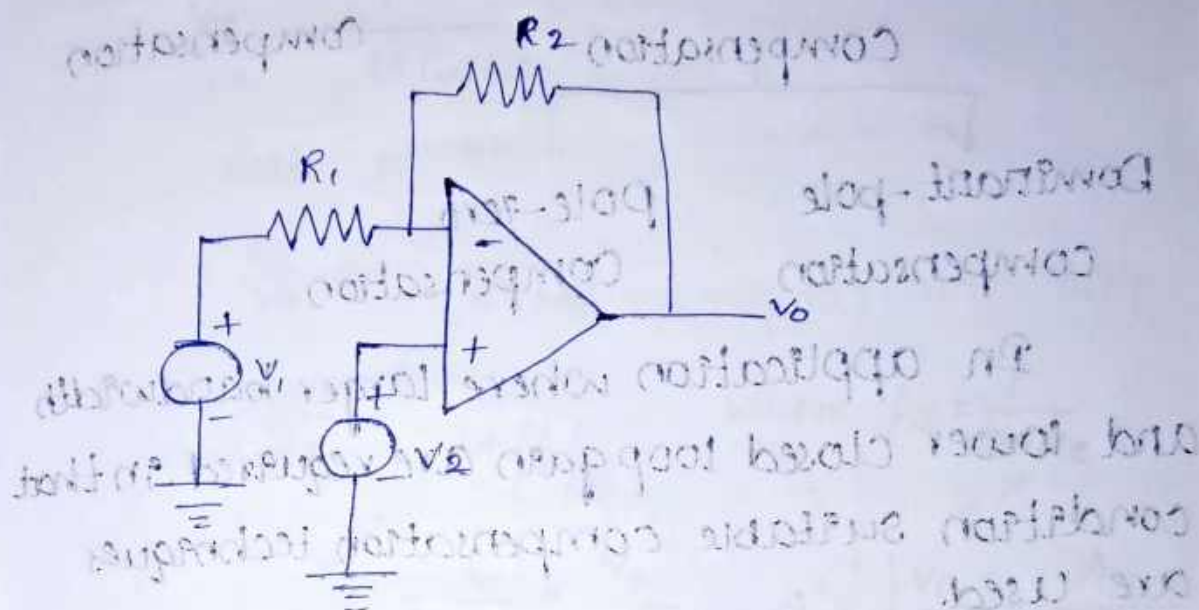


Fig:- Resistive feedback of an op-amp

This circuit is used as a inverting op-amp for $V_2 = 0$ and non-inverting op-amp for $V_1 = 0$.

For negative feedback concept the closed loop transfer function

$$A_{CL} = \frac{A}{1 + A\beta}$$

where, A = open loop gain
 β = feedback ratio

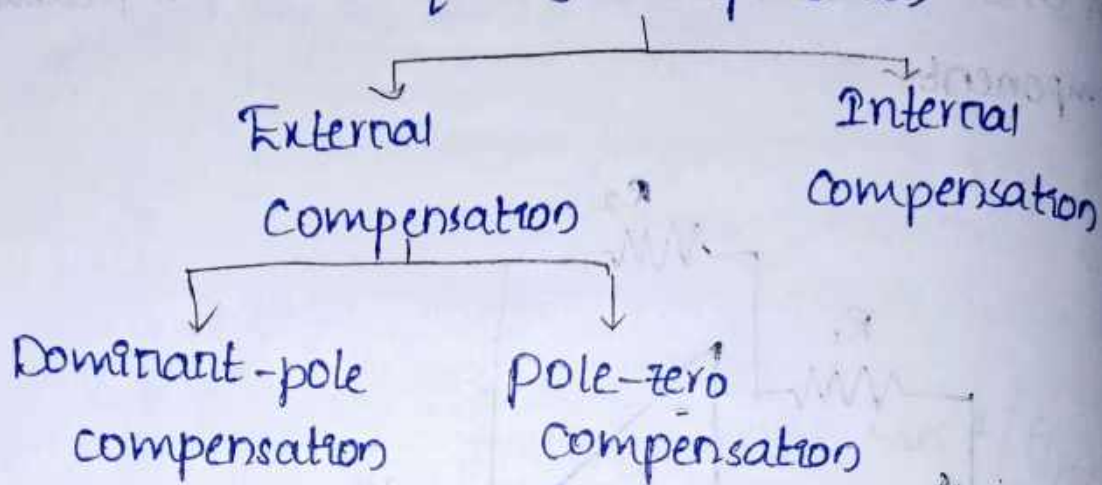
$$|A\beta| \geq 1$$

$$\theta = 0^\circ \text{ or } 360^\circ \frac{V}{V} = \frac{V}{V}$$

$$\frac{(\frac{1}{s\omega})}{(\frac{1}{s\omega} + 1)} \times V = 0V$$

Frequency compensation

Frequency compensation



In application where larger bandwidth and lower closed loop gain are required in that condition suitable compensation techniques are used.

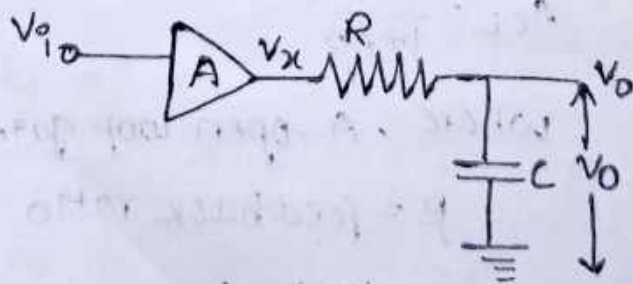
External frequency Compensation:-

Some type of op-amps are made to be used with externally compensating components.

Types of External frequency compensation:-

- 1) Dominant pole compensation
- 2) Pole-zero compensation.

1) Dominant pole compensation



$$\frac{V_o}{V_i} = \frac{V_o}{V_x} \cdot \frac{V_x}{V_i}$$

$$V_o = \frac{V_x \left(\frac{1}{j\omega C} \right)}{\left(R + \frac{1}{j\omega C} \right)}$$

$$\frac{V_o}{V_x} = \frac{\left(\frac{1}{j\omega C} \right)}{\left(\frac{Rj\omega C + 1}{j\omega C} \right)}$$

$$\frac{V_o}{V_x} = \frac{1}{1 + j\omega RC}$$

Sub $\omega = 2\pi f$

$$\frac{V_o}{V_x} = \frac{1}{1 + j2\pi f RC}$$

$$\frac{V_o}{V_x} = \frac{1}{1 + \left(j \frac{f}{f_d} \right)} \quad \text{where } f_d = \frac{1}{2\pi RC}$$

$$\frac{V_o}{V_i} = \frac{V_o}{V_x} \times \frac{V_x}{V_i} \Rightarrow A' = \left| \frac{V_o}{V_i} \right| = \frac{A}{\sqrt{1 + \left(\frac{f}{f_d} \right)^2}}$$

$$A' = \frac{V_o}{V_i} = \frac{A}{\left(1 + j \frac{f}{f_d} \right)}$$

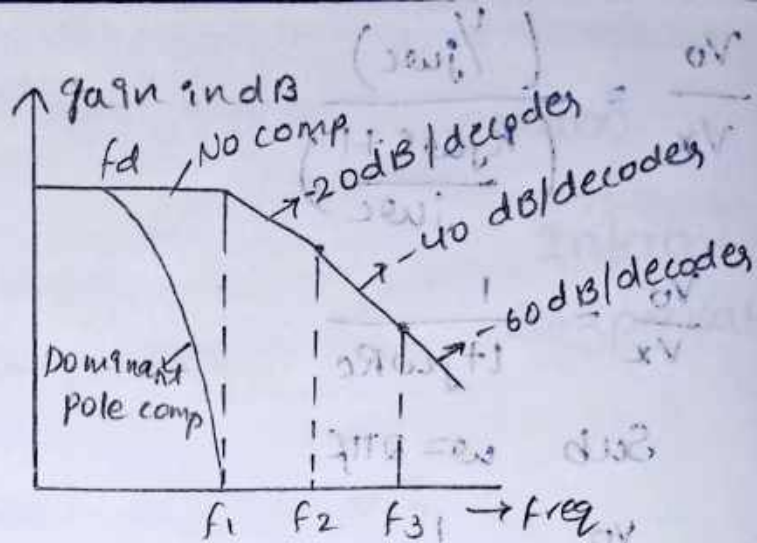
'A' is the uncompensated in a op-amp of open loop gain in this by adding a RC Network in series with the op-amp.

$$\text{Now } A' = \frac{V_o}{V_i} = \frac{A}{\left(1 + j \frac{f}{f_d} \right)}$$

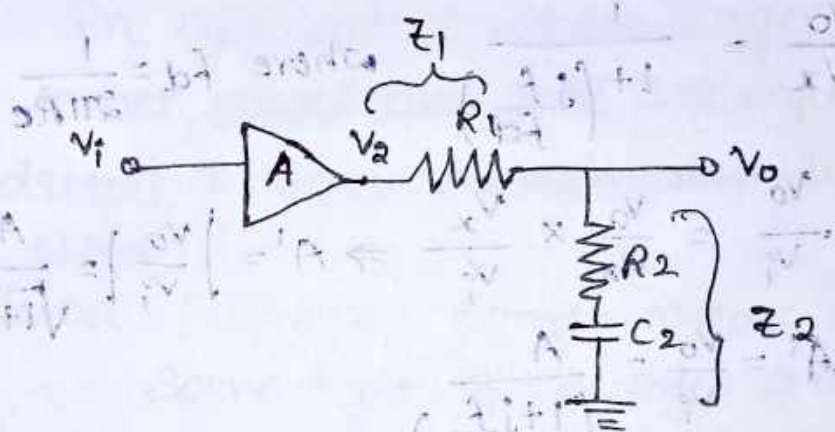
where A' is the compensated transfer function for 3 corner frequency.

$$A' = \frac{A_{OL}}{\left(1 + j \frac{f}{f_d} \right) \left(1 + j \frac{f}{f_{c1}} \right) \left(1 + j \frac{f}{f_{c2}} \right) \left(1 + j \frac{f}{f_{c3}} \right)}$$

$$\left(\frac{1}{20000 + j20000} \right) \text{ dB}$$



pole-zero compensation



Here the uncompensated transfer function is altered by adding both pole-zero as shown in figure.

The transfer function-compensated Network is

$$\frac{V_o}{V_i} = \frac{V_o}{V_2} \times \frac{V_2}{V_i}$$

$$V_o = \frac{z_2}{z_2 + z_1}$$

$$= \frac{V_2 \left(R_2 + \frac{1}{s\omega C_2} \right)}{\left[\left(R_2 + \frac{1}{j\omega C_2} \right) + R_1 \right]}$$

$$V_2 = \frac{V_0 \left[R_2 + \frac{1}{j\omega C_2} \right]}{\left[(R_1 + R_2) + \frac{1}{j\omega C_2} \right]}$$

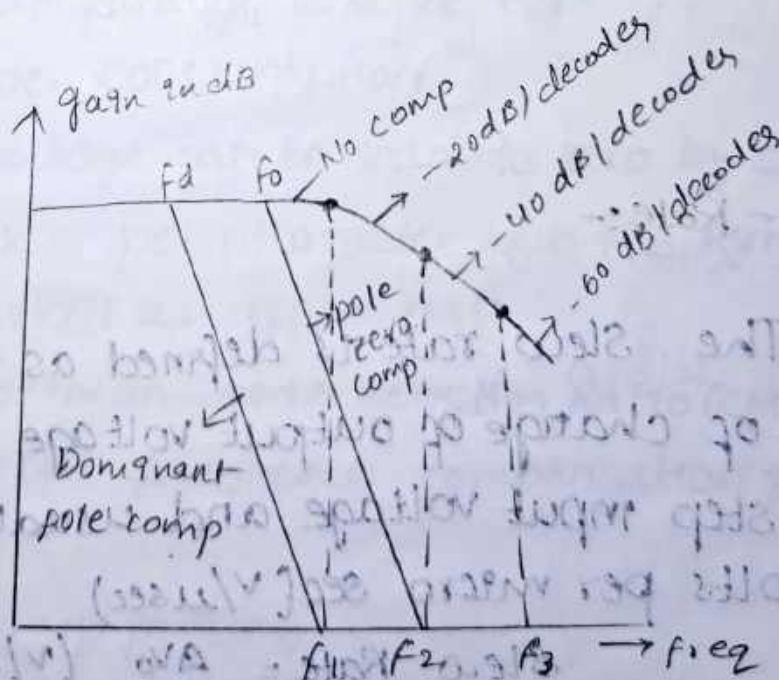
$$\frac{V_0}{V_2} = \frac{R_2}{R_1 + R_2} \left(\frac{1 + \frac{1}{j\omega R_2 C_2}}{1 + \frac{1}{j\omega (R_1 + R_2) C_2}} \right)$$

Substitute $\omega = 2\pi f$

$$\frac{V_0}{V_2} = \left(\frac{R_2}{R_2 + R_1} \right) \frac{\left(1 + \frac{1}{j 2\pi f R_2 C_2} \right)}{\left(1 + \frac{1}{j 2\pi f (R_1 + R_2) C_2} \right)}$$

$$\frac{V_0}{V_2} = \frac{R_2}{R_2 + R_1} \frac{\left(1 + \frac{f_1}{jf} \right)}{\left(1 + \frac{f_0}{jf} \right)} \quad \text{where } f_1 = \frac{1}{2\pi R_2 C_2}$$

$$A' = A \left(\frac{R_2}{R_2 + R_1} \right) \frac{\left(1 + \frac{f_1}{jf} \right)}{\left(1 + \frac{f_0}{jf} \right)} \quad f_0 = \frac{1}{2\pi (R_1 + R_2) C_2}$$

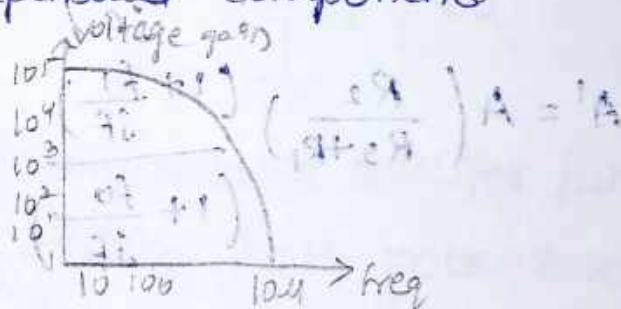


Comparison between pole-zero & Dominant pole compensation

Internally Compensated Op-amp

Sometimes relatively broad bandwidth of the uncompensated op-amp is not needed. Ex:- In the instrumentation circuit the op-amp is required to amplify relatively slow changing signals and therefore it doesn't require good high frequency response.

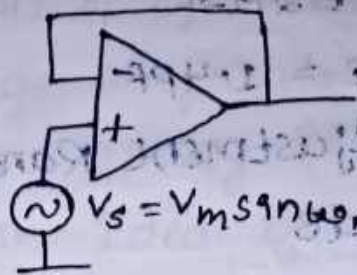
In this condition and similar applications we are using internally compensated op-amp. They are also called compensated op-amp. They are stable regardless of the value of closed loop gain and without externally connected compensated components.



Slew - Rate:-

The Slew rate is defined as the max rate of change of output voltage caused by the step input voltage and usually specified in volts per micro sec ($V/\mu\text{sec}$)

$$\text{Slew Rate} = \frac{\Delta V_o}{\Delta t} \text{ (V}/\mu\text{sec)}$$



$$V_s = V_m \sin \omega t$$

$$V_o = V_m \sin \omega t$$

$$SR = \left. \frac{dV_o}{dt} \right|_{\max} = \left. \frac{d}{dt} (V_m \sin \omega t) \right|_{\max}$$

$$= V_m \cos \omega t \cdot \omega \big|_{\max}$$

$$= V_m (1) 2\pi f$$

$$SR = \frac{2\pi f V_m}{10^6} \left(\frac{V}{\mu\text{sec}} \right)$$

Features of 741 Op-amp:-

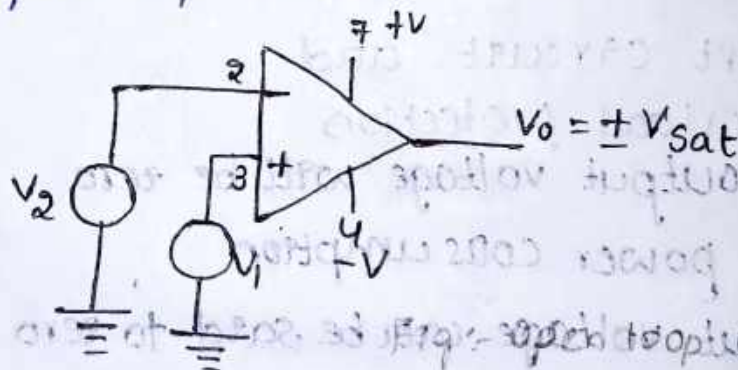
- 1) Short circuit and overload protection
- 2) Dc output voltage will be zero
- 3) Low power consumption
- 4) Output voltage can be said to zero by connecting $10k\Omega$ potentiometer b/w the terminals and marked as offset null.
- 5) Large common Mode Rejection Ratio (CMRR)
- 6) No external frequency compensation is required.
- 7) No latch up problem
- 8) Input offset voltage = $20mV$ & Input offset current = $20-200nA$ & Input bias current = $80-500nA$

- 9) Input Resistance = $2\text{ M}\Omega$
- 10) Input Capacitance = 1.4 pF
- 11) Offset voltage adjustment Range = $\pm 15\text{ mV}$
- 12) CMRR = 70 to 90 dB
- 13) Supply Voltage Rejection Ratio (SVRR) = $30-150$
- 14) Slew Rate = $0.5\text{ V}/\mu\text{sec}$
- 15) Output Resistance = 75Ω
- 16) Output voltage Swing = ± 10 to $\pm 13\text{ V}$
- 17) large signal voltage gain = 2×10^5

Modes of Operation

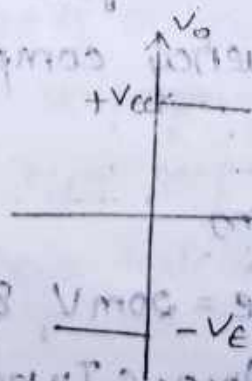
1. Open loop Operation of Op-amp.

The simplest way to use an op-amp is in open loop mode



1) When $V_2 > V_1 \Rightarrow V_0 = -V_{\text{sat}}$

2) When $V_2 < V_1 \Rightarrow V_0 = +V_{\text{sat}}$



Ideal characteristics of an op-amp under open-loop mode

Application of open-loop Op-Amp

1, voltage comparator

2, zero crossing Detector

3, Feedback in Ideal Op-amp

The utility of an Op-amp can be greatly increase by providing negative feedback. The output in this case not driven in the saturation and the circuit behaves in linear manner.

The two assumptions to simplify the mathematical calculations

$$I^+ = 0 \text{ \& } I^- = 0$$

The current drawn by either of the input terminals (inverting or non-inverting) will be negligible.

$$V_d = 0$$

The differential voltage V_d between inverting and non-inverting is essentially zero.



(3) Inverting amplifier

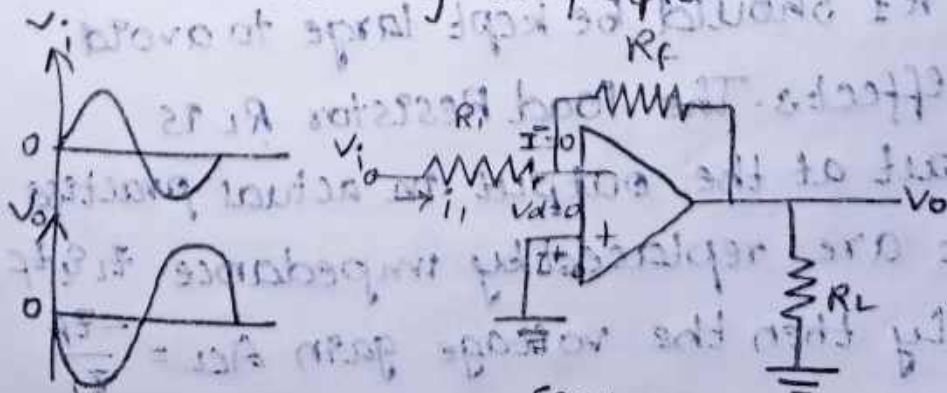


Fig:- Inverting Amplifier

$$\frac{V_a - V_i}{R_i} + \frac{V_a - V_o}{R_f} = 0 \quad \text{--- (1)}$$

$V_d = 0$ for Ideal op-amp

$$V_d = (V_+) - (V_-)$$

$$V_+ = \text{GND}$$

$$0 = 0 - (V_-)$$

$$(V_-) = 0 = V_a$$

Substitute V_a in equation (1)

$$\frac{-V_i}{R_i} + \frac{V_o}{R_f} = 0$$

$$V_o = -\frac{R_f}{R_i} V_i ; \text{gain } A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

In this circuit the input voltage V_i (ac/dc) is applied to the inverting input terminal through R_i and non-inverting terminal of the op-amp is grounded.

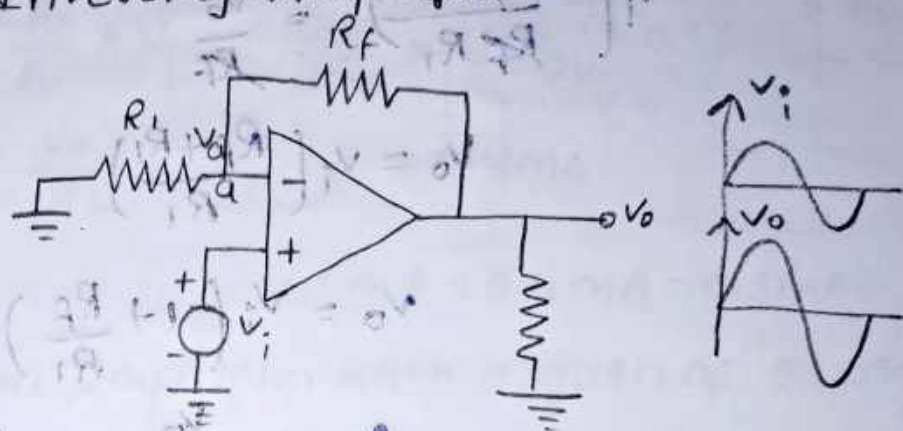
→ The negative sign in gain indicates phase shift 180° in between V_i & V_o . Since the input terminal is at virtual ground ($V_a = 0$).

→ The effective input impedance is R_i . The value of R_i should be kept large to avoid loading effects. The load Resistor R_L is usually put at the output in actual practice.

→ If R_i & R_f are replaced by impedance Z_i & Z_f respectively then the voltage gain $A_{CL} = -\frac{Z_f}{Z_i}$

The above formulae we can use in integrator, differentiator etc --

4, Non-Inverting Amplifier



If a signal (ac or dc) is applied to the non-inverting input terminal and feedback is as given as shown in figure. This circuit amplifies without inverting the input signal.

This is called Non-Inverting amplifier.

→ The output voltage is in phase with the input voltage.

$$\frac{V_a - V_o}{R_1} + \frac{V_a - V_o}{R_f} = 0 \quad (1)$$

$V_d = 0$ for an Ideal op-amp

$$V_d = (V_+) - (V_-)$$

$$V_+ = V_i$$

$$0 = V_i - (V_-)$$

$$V_- = V_i$$

$$V_a = V_i$$

Substitute $V_a = V_i$ in eq (1)

$$\frac{V_i}{R_1} + \frac{V_i - V_o}{R_f} = 0$$

$$V_i \left(\frac{1}{R_i} + \frac{1}{R_f} \right) = \frac{V_o}{R_f}$$

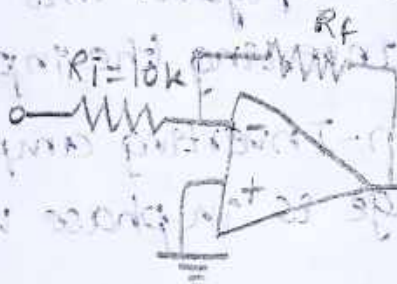
$$V_i \left(\frac{R_f + R_i}{R_f R_i} \right) = \frac{V_o}{R_f}$$

$$V_o = V_i \left(\frac{R_f + R_i}{R_i} \right)$$

$$V_o = V_i \left(1 + \frac{R_f}{R_i} \right)$$

$$A_{CL} = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_i}$$

Design an Amplifier with a gain of -10 and Input Resistance = $10k\Omega$



$$A = -10, R_i = 10k\Omega$$

$$A_{CL} = \frac{-R_f}{R_i}$$

$$-10 = \frac{-R_f}{10k}$$

$$R_f = 100k\Omega$$

In an amplifier $R_i = 10k\Omega$, $R_f = 100k\Omega$, $V_i = 1V$. A load of $25k\Omega$ is connected to the output terminal. Calculate i_i , V_o , i_L , i_o in inverting amplifier.

$$R_i = 10k\Omega$$

$$R_f = 100k\Omega$$

$$V_i = 1V$$

$$i_i = \frac{V_i}{R_i} = \frac{1V}{10k} = 0.1\mu A$$

$$R_L = 25k\Omega$$

$$i) i_1 = \frac{V_1}{R_1} = \frac{1}{10k} = 0.1mA$$

$$ii) V_o = -\frac{R_f}{R_1} \times V_i = -\frac{100k}{10k} \times 1 = -10V$$

$$iii) i_L = \frac{V_o}{R_L} = \frac{10}{25k\Omega} = 0.4mA$$

$$iv) i_o = i_1 + i_L = 0.1mA + 0.4mA = 0.5mA$$

Design an amplifier with a gain of 5 using op-amp.

$$A_{CL} = 1 + \frac{R_f}{R_1}$$

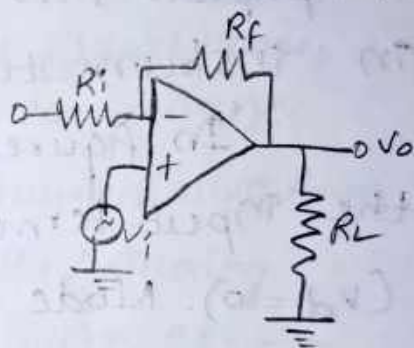
$$\text{Assume } R_1 = 10k\Omega$$

$$5 = 1 + \frac{R_f}{10k}$$

$$5 - 1 = \frac{R_f}{10k}$$

$$4 = \frac{R_f}{10k}$$

$$R_f = 40k\Omega$$



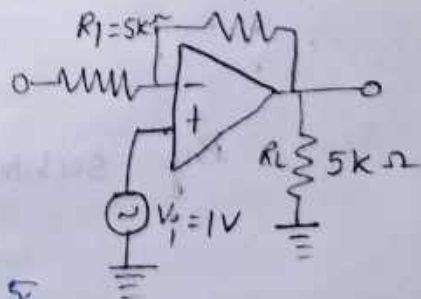
In the circuit. $R_1 = 5k\Omega$, $R_f = 20k\Omega$ & $V_i = 1V$ a load Resistor of $5k\Omega$ is connected at the output as shown in the figure. Calculate V_o , A_{CL} , I_o , I_L .

$$V_o = V_i \left(1 + \frac{R_f}{R_1} \right) = 1 \left(1 + \frac{20k}{5k} \right) = 5V$$

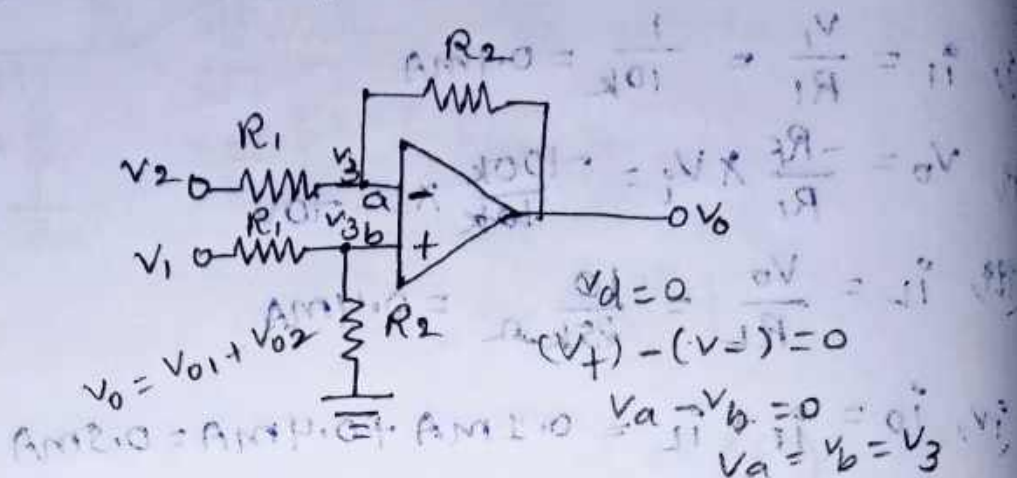
$$A_{CL} = \frac{5}{1} = 5$$

$$I_o = I_1 + I_L = 0.2mA + 1mA = 1.2mA \quad I_L = \frac{V_o}{R_L} = \frac{5}{5k} = 1mA$$

$$I_1 = \frac{V_i}{R_1} = \frac{1}{5k} = 0.2mA$$



Differential Amplifier



The circuit that amplifies difference between the two signals is called differential amplifier. This type of amplifiers very useful in instrumentation circuit.

In figure the differential voltage at the input terminal of the op-amp is zero ($V_d = 0$). Node a & Node b are at the same potential designated / marked as V_3 .

The nodal equation at node a.

$$\frac{V_3 - V_2}{R_1} + \frac{V_3 - V_0}{R_2} = 0$$

$$V_3 \left(\frac{1}{R_1} + \frac{1}{R_2} \right) - \frac{V_2}{R_1} - \frac{V_0}{R_2} = 0 \quad (1)$$

The nodal equation at node 'b'.

$$\frac{V_3 - V_1}{R_1} + \frac{V_3 - 0}{R_2} = 0$$

$$V_3 \left(\frac{1}{R_1} + \frac{1}{R_2} \right) - \frac{V_1}{R_1} = 0 \quad (2)$$

By subtraction of (1) & (2)

$$\frac{V_1}{R_1} - \frac{V_2}{R_1} = \frac{V_0}{R_2}$$

$$\frac{V_1 - V_2}{R_1} = \frac{V_0}{R_2}$$

$$V_0 = \frac{R_2}{R_1} (V_1 - V_2)$$

This circuit is very useful in detecting very small difference in input signal. Since the gain R_2/R_1 , can be chosen to be very large.

Op-Amp Applications:-

1. Op-Amp has countless applications and forms the basic building block of the linear & non-linear analog systems.

Linear Circuit:- The output signal varies with the ip signal in a linear manner.

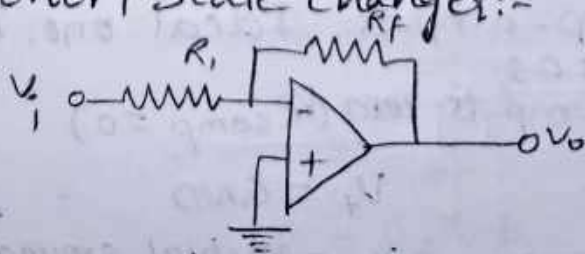
Ex:- Adder, Subtractor, Instrumentation Amp, V-I Converter, I-V Converter, Analog Computation, power amplifiers, etc---

Non-linear Circuit:- The output signal with the input signal in a non-linear manner.

Ex:- Rectifiers, Peak detector, Clippers, clammers, Sample and Hold circuit, log and anti-log amplifiers, multipliers, etc---

These non-linear circuits very useful in industrial instrumentation, communication system, general signal processing system

Inverter / Scale changes:-



The above CKT can be used as an Inverter by keeping $R_f = R_i$.

The above circuit can be used as a scalar changer by keeping $R_f/R_i = \text{const}$ value (k).

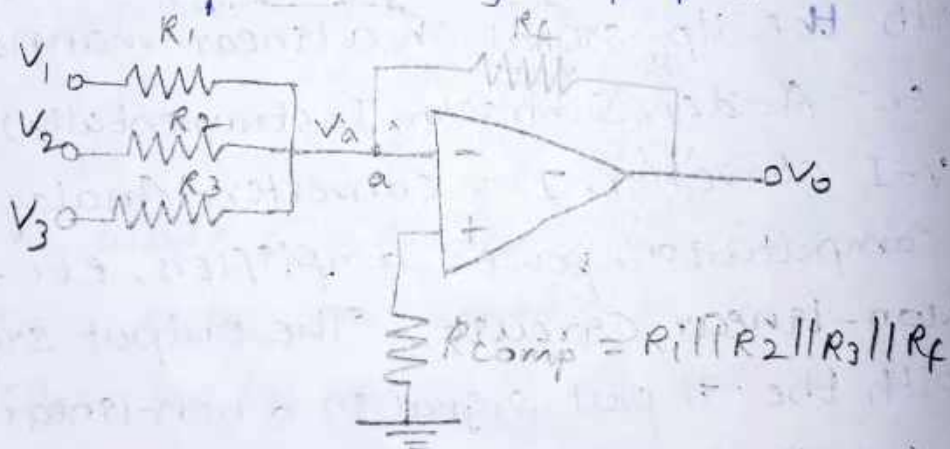
$$V_o = -\frac{R_f}{R_i} V_i \quad V_o = -\frac{R_f}{R_i} R V_i$$

$$V_o = -V_i$$

$$V_o = -k V_i$$

Summing Amplifiers:-

1. Inverting Summing Amplifier



Write the nodal equation at node "a".
Voltage at that node is " V_a ".

$$\frac{V_a - V_1}{R_1} + \frac{V_a - V_2}{R_2} + \frac{V_a - V_3}{R_3} + \frac{V_a - V_o}{R_f} = 0$$

$$V_a \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_f} \right) - \frac{V_1}{R_1} - \frac{V_2}{R_2} - \frac{V_3}{R_3} = \frac{V_o}{R_f}$$

Assume op-amp is Ideal one, i.e.,
offset voltage = 0;
voltage at R_{comp} is zero ($V_{comp} = 0$)

$$V_+ = \text{GND}$$

$$V_- = \text{Virtual ground}$$

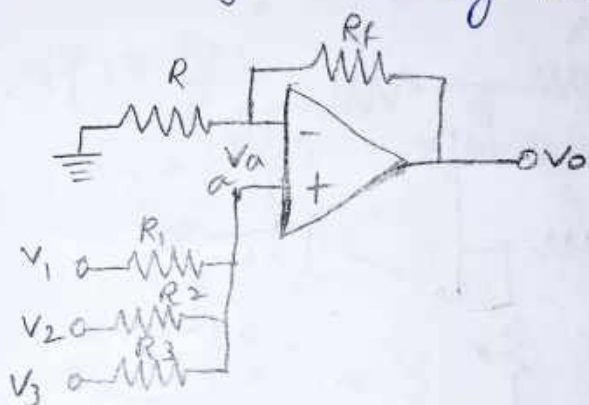
$$V_0 = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

$$\text{Let } R_1 = R_2 = R_3 = R_f = R$$

$$\begin{aligned} V_0 &= -R \left(\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R} \right) \\ &= -R \left(\frac{V_1 + V_2 + V_3}{R} \right) \end{aligned}$$

$$\boxed{V_0 = -(V_1 + V_2 + V_3)}$$

2, Non-Inverting summing Amplifier.



$$V_0 = V_+ \left(1 + \frac{R_f}{R} \right)$$

$$\frac{V_a - V_1}{R_1} + \frac{V_a - V_2}{R_2} + \frac{V_a - V_3}{R_3} = 0$$

$$V_a = \frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)}{\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right)}$$

$$\boxed{V_0 = V_a \left(1 + \frac{R_f}{R} \right)}$$

$$V_0 = \frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right) \left(1 + \frac{R_f}{R} \right)}{\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right)}$$

$$R_1 = R_2 = R_3 = R$$

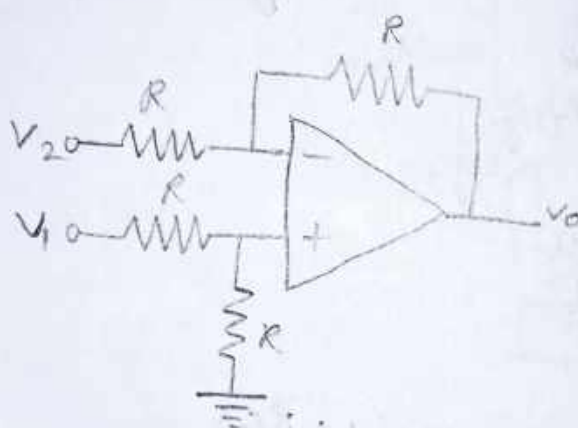
$$R_f = 2R$$

$$V_o = \frac{\left(\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R} \right)}{\left(\frac{1}{R} + \frac{1}{R} + \frac{1}{R} \right)} \left(1 + \frac{2R}{R} \right)$$

$$= \frac{\left(\frac{V_1 + V_2 + V_3}{R} \right)}{\left(\frac{3}{R} \right)} \quad (3)$$

$$V_o = V_1 + V_2 + V_3$$

Subtractor:-



$$V_{o2} = \frac{-R}{R} \times V_2 = -V_2$$

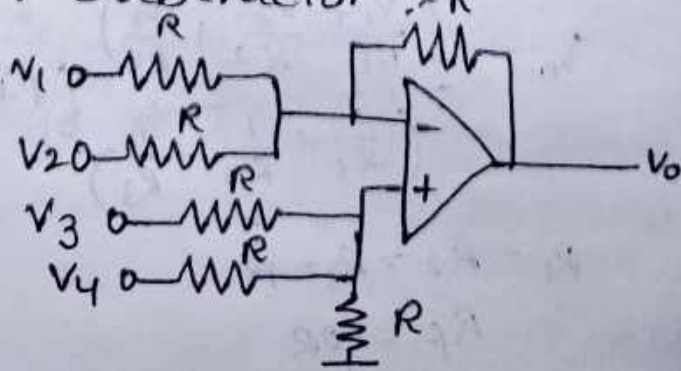
$$V_{o1} = \left(1 + \frac{R}{R} \right) V_+ = 2 \left(\frac{V_1}{2} \right) = V_1$$

$$V_+ = V_1 \times \frac{R}{R+R} = V_1 \frac{R}{2R} = \frac{V_1}{2}$$

$$V_o = V_{o1} + V_{o2}$$

$$V_o = V_1 - V_2$$

Adder-Subtractor :-



$$V_o = V_{o1} + V_{o2} + V_{o3} + V_{o4}$$

$$V_{o1} \text{ due to } V_1 \text{ \& } V_2 = V_3 = V_4 = 0$$

$$V_{o1} = -\frac{R_f}{R} (V_i)$$

$$= -\frac{R}{R/2} \left(\frac{V_1}{2} \right)$$

$$= -2 \left(\frac{V_1}{2} \right)$$

$$V_{o1} = -V_1$$

$$\text{Similarly } V_{o2} = -V_2$$

$$V_{o3} = V_3 \left(1 + \frac{R_f}{R} \right)$$

$$V_4 = V_3 \times \frac{(R/2)}{\left(\frac{R}{2} + R \right)}$$

$$= \frac{V_3 \left(\frac{R}{2} \right)}{\frac{3R}{2}} = \frac{V_3}{3}$$

$$= \frac{V_3}{3} \left(1 + \frac{R}{R/2} \right) \Rightarrow \frac{V_3}{3} \left(1 + \frac{R}{1} \times \frac{2}{R} \right)$$

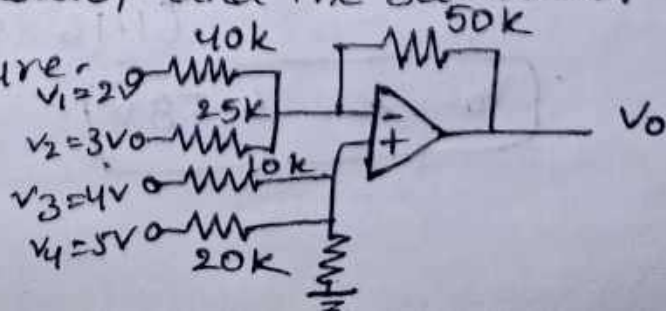
$$V_{o3} = \frac{V_3}{3} (3) \Rightarrow \frac{V_3}{3} (3)$$

$$V_{o3} = V_3$$

$$\text{Similarly } V_{o4} = V_4$$

$$V_o = (V_3 + V_4) - (V_1 + V_2)$$

Find V_o for adder and the subtractor which shown in figure.



$$V_0 = V_{01} + V_{02} + V_{03} + V_{04}$$

Inverting $V_0 = -\frac{R_f}{R_1} V_1 - \frac{R_f}{R_2} V_2$

$$= -\frac{50k}{40k} (V_1) - \frac{50k}{25k} (V_2)$$

$$V_0 = -1.25 V_1 - 2 V_2$$

Non-Inverting

$$V_0 = \left(1 + \frac{R_f}{R_1}\right) V_+$$

$$V_+ = V_3 \left[\frac{(20k \parallel 30k)}{(20k \parallel 30k) + 10k} \right]$$

$$V_+ = V_4 \left[\frac{10k \parallel 30k}{(10k \parallel 30k) + 20k} \right]$$

$$V_0 = \left[1 + \frac{50k}{40k \parallel 25k} \right] \left[V_3 \frac{(20k \parallel 30k)}{(20k \parallel 30k) + 10k} + \right.$$

$$\left. V_4 \frac{10k \parallel 30k}{(10k \parallel 30k) + 20k} \right]$$

$$= \left(1 + \frac{50k}{15.38k} \right) \left[V_3 \left(\frac{12k}{12k + 10k} \right) + V_4 \left(\frac{7.5k}{7.5k + 20k} \right) \right]$$

$$= \left(1 + \frac{50k}{15.38k} \right) (0.545 V_3 + 0.273 V_4)$$

$$V_0 = 2.32 V_3 + 1.16 V_4$$

$$V_0 = -1.25 V_1 - 2 V_2 + 2.32 V_3 + 1.16 V_4$$

$$= (-1.25 \times 2V) - (2 \times 3) + (2.32 \times 4)$$

$$(1.16 \times 5)$$

$$V_0 = 6.58V$$

CMRR (Common mode Rejection Ratio):

The relative sensitivity of an op-amp to difference signal as compared to common mode signal is called CMRR and it is represented as ρ (figure of merit).

$$\rho = \left| \frac{A_{DM}}{A_{CM}} \right| \text{ dB}$$

For $\mu A 741$ op-amp has minimal CMRR of 70 dB

$$A_{DM} = \frac{A_1 - A_2}{2}$$

$$A_{CM} = A_1 + A_2$$

For Better op-amp, CMRR value must be high. Ratio of differential mode gain to common mode gain is called CMRR.

SVRR (PSRR, PSS) (Supply voltage Rejection

Ratio / Power Supply Rejection Ratio / power supply sensitivity)

The change in op-amp input offset voltage due to variation in supply voltage is called SVRR. This expressed in terms of $\mu V/V$ (or) in decibels:

$$\text{For } 741C \text{ SVRR} = \pm 50 \mu V/V$$

For better op-amp, SVRR should be lower value.

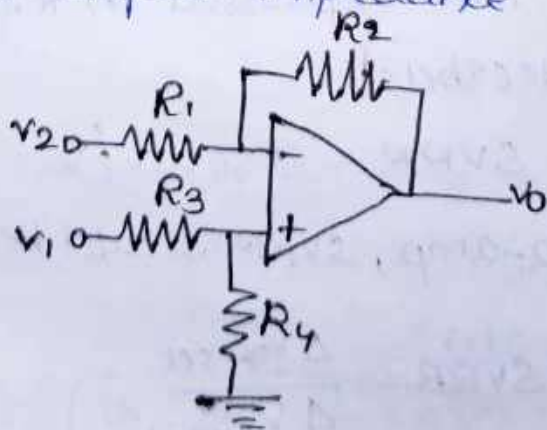
$$SVRR = \frac{\Delta V_{\text{offset}}}{\Delta V_{\text{supply}}}$$

Instrumentation Amplifier:-

This amplifier is used in industrial and consumer applications to measure and control physical quantities. Physical quantities are humidity, Light intensity, water flow, temperature etc. These physical quantities are usually measured with the help of transducers. The output of the transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier.

→ Important features of Instrumentation amplifier are:-

- 1) High gain accuracy.
- 2) High gain CMRR
- 3) High gain stability with low temperature coefficient.
- 4) Low dc offset
- 5) Low output impedance



Fig(a): Differential amplifier using single op-amp

$$V_0 = V_{02} + V_{01}$$

$$= -V_2 \frac{R_2}{R_1} + V_1 \times \frac{R_4}{R_4 + R_3} \left(1 + \frac{R_2}{R_1} \right)$$

$$= -V_2 \frac{R_2}{R_1} + V_1 \frac{1}{\left(1 + \frac{R_3}{R_4} \right)} \left(1 + \frac{R_2}{R_1} \right)$$

$$= -\frac{R_2}{R_1} \left[V_2 - \frac{V_1}{\left(1 + \frac{R_3}{R_4} \right)} \left(\frac{R_1}{R_2} + 1 \right) \right]$$

$$\text{For } \frac{R_1}{R_2} = \frac{R_3}{R_4}$$

$$V_0 = -\frac{R_2}{R_1} \left[V_2 - \frac{V_1}{\left(1 + \frac{R_3}{R_4} \right)} \left(\frac{1 + \frac{R_1}{R_2}}{\frac{1 + \frac{R_3}{R_4}}{\frac{R_1}{R_2}}} \right) \right]$$

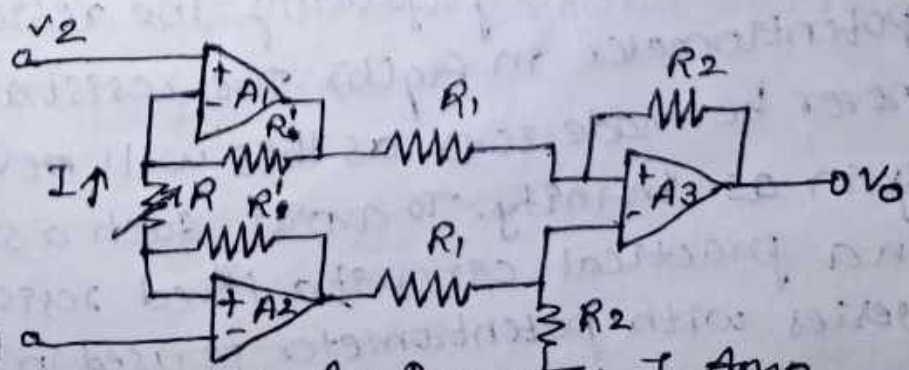
$$= -\frac{R_2}{R_1} [V_2 - V_1]$$

$$V_0 = \frac{R_2}{R_1} [V_1 - V_2]$$

In Fig (a), Source V_1 has an input impedance as $R_3 + R_4$.

Source V_2 has input impedance is R_1 .

This low impedance may load the signal source heavily. Therefore high resistance buffers is used at the preceeding states of each input to avoid the loading effect as shown in Fig(b).



Fig(b) :- An Improved I-Amp

1) When $V_1 = V_2$, $I = 0$, $V_R = 0$, $V_2' = V_2$, $V_1' = V_1$

$$\begin{aligned} V_0 &= -V_2' \cdot \frac{R_2}{R_1} + V_1' \cdot \frac{R_2}{R_2 + R_1} \left(1 + \frac{R_2}{R_1} \right) \\ &= -V_2' \cdot \frac{R_2}{R_1} + V_1' \left(\frac{R_2}{R_2 + R_1} \right) \left(\frac{R_2 + R_1}{R_1} \right) \\ &= (-V_2' + V_1') \left(\frac{R_2}{R_1} \right) \end{aligned}$$

$$V_0 = \frac{R_2}{R_1} (V_1' - V_2')$$

2) when $V_1 \neq V_2$, $I = \frac{V_1 - V_2}{R}$

$$V_1' = IR' + V_1 = \left(\frac{V_1 - V_2}{R} \right) R' + V_1$$

$$V_2' = -IR' + V_2 = -\left(\frac{V_1 - V_2}{R} \right) R' + V_2$$

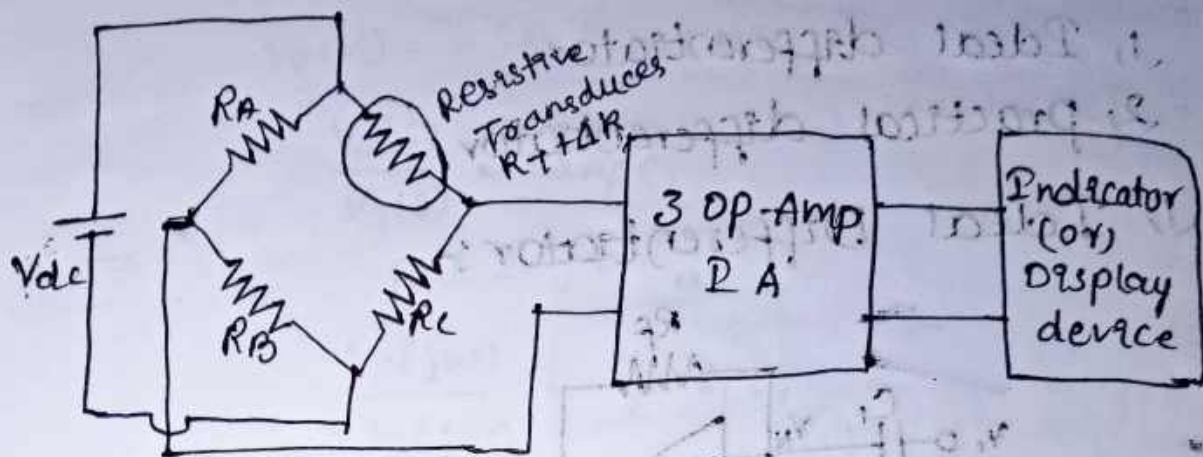
$$V_0 = \frac{R_2}{R_1} (V_1' - V_2')$$

$$= \frac{R_2}{R_1} \left[\left(\frac{V_1 - V_2}{R} \right) R' + V_1 + \left(\frac{V_1 - V_2}{R} \right) R' - V_2 \right]$$

$$= \frac{R_2}{R_1} \left[2 \left(\frac{V_1 - V_2}{R} \right) R' + (V_1 - V_2) \right]$$

$$V_0 = \frac{R_2}{R_1} (V_1 - V_2) \left[\frac{2R'}{R} + 1 \right]$$

→ The differential gain of instrumentation amplifier can be varied by replacing the resistance by potentiometer in fig(b). The resistance should never be made zero as this will never make gain as infinity. To avoid such a situation in a practical circuit a fixed resistance in series with potentiometer is used in place of R .



Fig(c):- Instrumentation amplifier using Transducer bridge

Fig(c) shows a differentiation instrumentation amplifier using transducer bridge. The circuit uses a resistive transducer whose resistance changes as a function of physical quantity to be measured.

The bridge is initially balanced by a dc supply voltage V_{dc} so that $V_1 = V_2$.

As physical quantity changes the resistive R_T of the transducer also changes causing an unbalanced in the bridge. So we get $V_1 \neq V_2$.

The differential voltage now gets amplified by the 3op-Amp Instrumentation amplifier. Finally the differential voltage we observe in the display device.

Differentiator :

- 1, Ideal differentiator
- 2, practical differentiator

1, Ideal Differentiator :

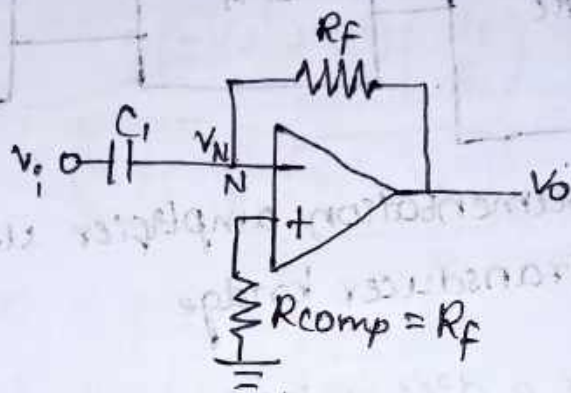


Fig (1)

The figure shows the differential amplifier as its name implies the circuit performs mathematical operation of differentiation i.e., output waveform is the derivative of the input waveform.

The differentiator may be constructed from the inverting amplifier if an input R_i is replaced by capacitor C_1 .

$$C_1 \frac{d(V_N - V_i)}{dt} + \frac{V_N - V_o}{R_f} = 0$$

Ideal op-amp characteristics

$$V_N = 0 \text{ (virtual ground)}$$

$$-C_1 \frac{dV_i}{dt} - \frac{V_o}{R_f} = 0$$

$$V_o = -R_f C_1 \frac{dV_i}{dt}$$

Laplace transform for the above eqn:

$$V_o(s) = -sR_f C_1 V_i(s)$$

$$\frac{V_o(s)}{V_i(s)} = -sR_f C_1$$

put $s = j\omega$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -j\omega R_f C_1$$

$$\omega = 2\pi f$$

$$= -j2\pi f R_f C_1$$

$$A = \frac{-jf}{f_a}$$

$$\text{where } f_a = \frac{1}{2\pi R_f C_1}$$

$$|A| = \frac{f}{f_a}$$

Thus, the output voltage V_o is a constant $(-R_f C_1)$ times the derivative of the input voltage and the minus sign indicates the 180° phase shift of the output waveform w.r.t the input signal. At $f = f_a$

$$|A| = 1$$

The gain increases at a rate of $+20\text{ dB}$ per decade. Thus at high frequencies a differentiator may become unstable and break into oscillation.

There is one more problem in the Fig(1) differentiator. The input impedance

$$Z_i = \frac{1}{2\pi f C_1} \text{ decreases}$$

with increase in frequency there by making

the circuit sensitive to the high frequency noise.

2. Practical differentiator.

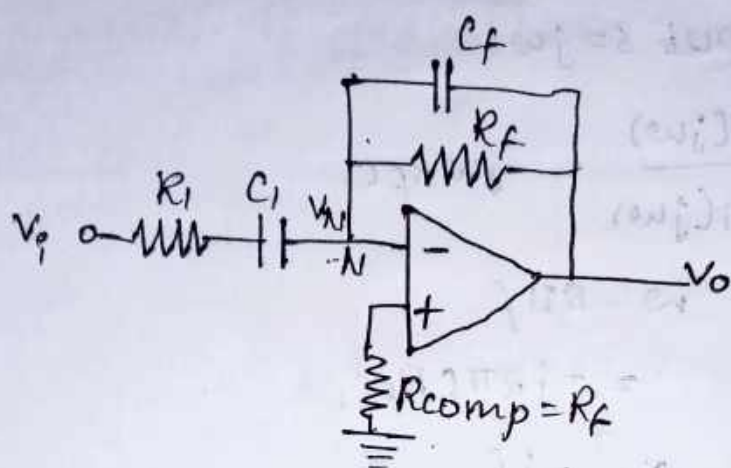


Fig (2) :-

Figure (2) shows the practical differentiator.

It eliminates the problem of stability (As frequency increases gain also increases) and high frequency noise (as frequency increases input impedance decreases).

$$V_o = -V_i \left(\frac{Z_f}{Z_i} \right)$$

$$\frac{V_o}{V_i} = \frac{-(R_f \parallel sC_f)}{\left(R_i + \frac{1}{sC_i} \right)}$$

$$= \frac{\left(\frac{R_f \times \frac{1}{sC_f}}{R_f + \frac{1}{sC_f}} \right)}{R_i + \frac{1}{sC_i}}$$

$$= \frac{\left[\frac{(R_f / sC_f)}{(sR_f C_f + 1) / sC_f} \right]}{\left[sR_i C_i + 1 \right] / sC_i}$$

$$\frac{V_o}{V_i} = \frac{-SR_f C_i}{(1 + R_f S C_f)(1 + SR_i C_i)}$$

$$\text{for } R_f C_f = R_i C_i$$

$$\frac{V_o}{V_i} = \frac{-SR_f C_i}{(1 + SR_f C_f)^2}$$

$$= \frac{-SR_f C_i}{(1 + j2\pi f R_f C_f)^2}$$

$$\frac{V_o}{V_i} = \frac{-SR_f C_i}{(1 + jf/f_b)^2} \rightarrow (2)$$

where

$$f_b = \frac{1}{2\pi R_f C_f}$$

⇒ From equation (2) for frequencies

$f < f_b$ the gain increases at a rate of $+20 \text{ dB/decade}$.

⇒ For frequency, $f > f_b$ the gain decreases at a rate of -20 dB/decade .

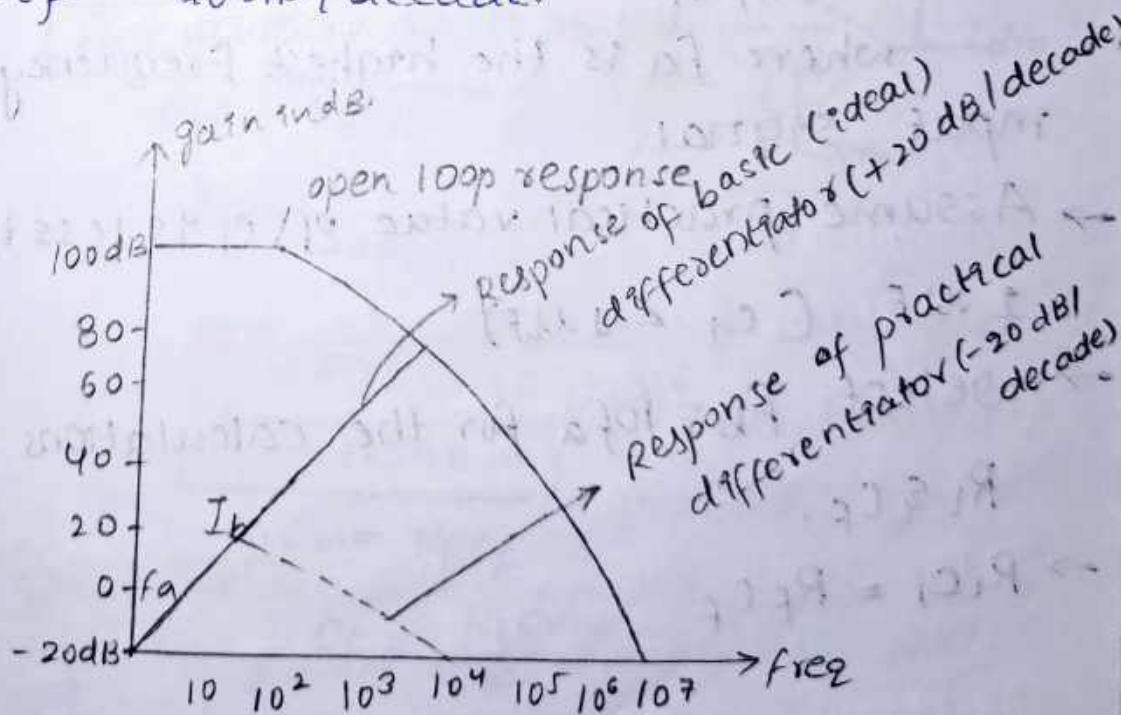


Fig (a): Frequency Response

For the basic differentiator of fig(a) the frequency response would have increase continuously at the rate of $+20\text{dB/decade}$ even beyond f_b causing stability problem at high frequency. So by using practical differentiator we reduce the gain at high frequency (dotted line shown in frequency response) and thereby avoiding stability problem and high frequency noise.

→ For a good differentiator the time period T of the input signal is larger or equal to $R_f C_1$ ($T \geq R_f C_1$)

$$\rightarrow R_f C_1 > R_i C_1 \\ > R_f C_f$$

$$\rightarrow f_a = \frac{1}{2\pi R_f C_1}$$

where f_a is the highest frequency of the input signal.

→ Assume practical value of C_1 is less than $1\mu\text{F}$ ($C_1 < 1\mu\text{F}$)

→ select $f_b = 10f_a$ for the calculations of R_i & C_f .

$$\rightarrow R_i C_1 = R_f C_f$$

A) Design an op-amp differentiator that will differentiate an input signal with $f_{\text{maximum}} = 100 \text{ Hz}$.
 B) Draw the output waveform for a sine wave of 1 Vp at 100 Hz applied to the differentiator.
 C) Repeat the part (B) for a square wave input.

$$f_{\text{max}} = 100 \text{ Hz} = f_a$$

$$C_1 < 1 \mu\text{F}$$

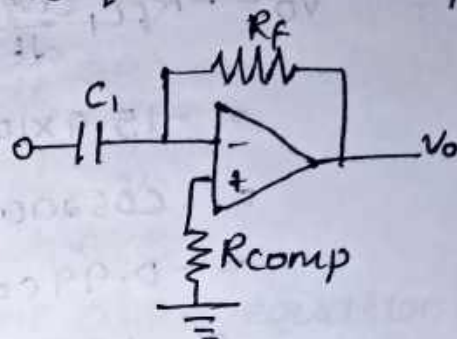
$$\therefore \text{Assume } C_1 = 0.1 \mu\text{F}$$

$$f_a = \frac{1}{2\pi R_f C_1}$$

$$100 = \frac{1}{2\pi R_f \times 0.1 \times 10^{-6}}$$

$$R_f = \frac{1}{2\pi \times 100 \times 0.1 \times 10^{-6}}$$

$$R_f = 15.9 \text{ k}\Omega$$



practical $f_b = 10 f_a$

$$f_b = 10 \times 100 = 1 \text{ kHz}$$

$$R_1 C_1 = R_f C_f$$

$$f_b = \frac{1}{2\pi R_1 C_1}$$

$$R_1 = \frac{1}{2\pi \times 10^3 \times 0.1 \times 10^{-6}}$$

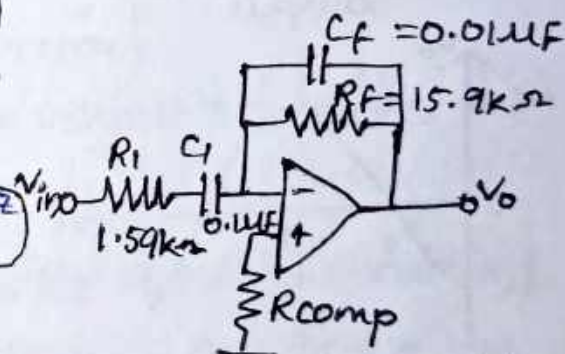
$$R_1 = 1.59 \text{ k}\Omega$$

$$R_1 C_1 = R_f C_f$$

$$C_f = \frac{R_1 C_1}{R_f}$$

$$= \frac{1.59 \times 10^3 \times 0.1 \times 10^{-6}}{15.9 \times 10^3}$$

$$C_f = 0.01 \mu\text{F}$$



B) $V_{in} = V_m \sin \omega t$
 $= V_m \sin 200\pi t$
 $= 15 \sin 200\pi t$

$V_{in} = \sin 200\pi t$

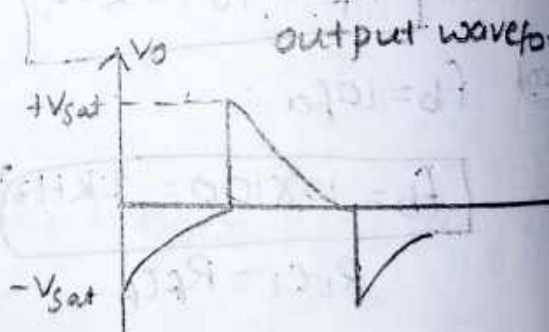
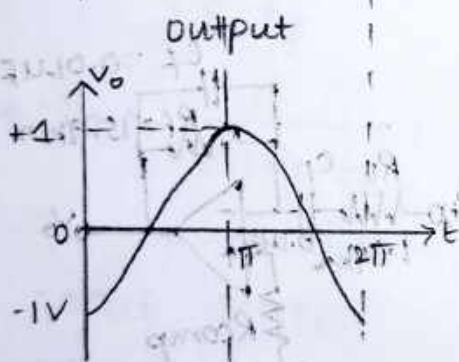
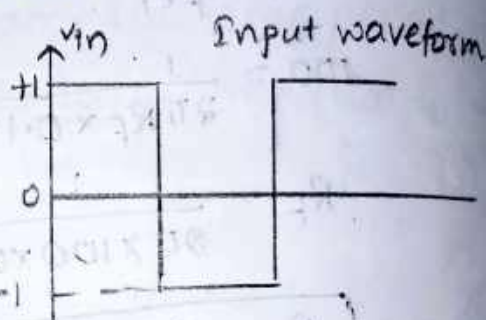
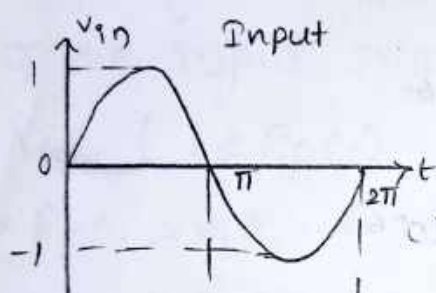
$V_o = -R_f C_1 \frac{dV_i}{dt}$

$= -15 \times 10^3 \times 0.1 \times 10^{-6} \frac{d}{dt} \sin(200\pi t)$

$= -\cos 200\pi t \times 200\pi$

$= -0.99 \cos 200\pi t$

$\approx -1 \cos 200\pi t$



Integrator :-

1) Ideal (or) Basic Integrator

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator. Such a CKT is obtained by using basic inverting amplifier configuration. If the feedback resistor is



by capacitor C_f .

$$\frac{V_N - V_i}{R_1} + C_f \frac{d(V_N - V_o)}{dt} = 0$$

$V_N = 0$ for an ideal op-amp

$$-\frac{V_i}{R_1} = C_f \frac{dV_o}{dt}$$

$$\frac{dV_o}{dt} = -\frac{1}{R_1 C_f} V_i$$

Integrating the above equation on both sides

$$V_o = -\frac{1}{R_1 C_f} \int V_i dt$$

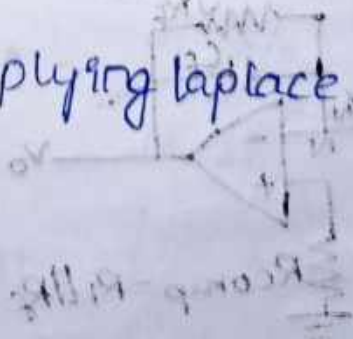
Now the output voltage is proportional to the time integral of the input where $R_1 C_f$ is the time constant of the integrator.

The negative sign in the output indicates the integrator is an inverting integrator.

The resistor R_{comp} is R_1 usually connected to the positive input terminal to minimize the effect of input bias current.

A simple low pass RC circuit can also work as integrator when time constant is very large.

By Applying Laplace transform



$$V_o(s) = \frac{-1}{R_1 C_f} \frac{V_{in}(s)}{s}$$

$$\frac{V_o(s)}{V_{in}(s)} = \frac{-1}{s R_1 C_f}$$

$$\text{put } s = j\omega$$

$$\frac{V_o(j\omega)}{V_{in}(j\omega)} = \frac{-1}{j\omega R_1 C_f}$$

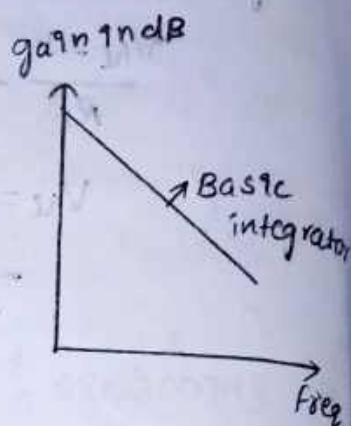
$$\text{Substitute } \omega = 2\pi f$$

$$= \frac{-1}{j 2\pi f R_1 C_f}$$

$$= \frac{-f_b}{j f}$$

$$\text{where } f_b = \frac{1}{2\pi R_1 C_f}$$

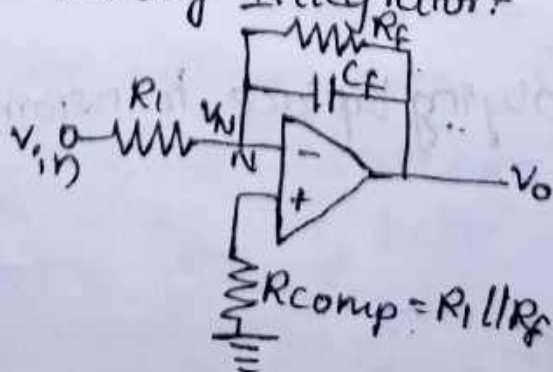
$$|A| = \frac{f_b}{f}$$



As the gain of the integrator decreases with the increase in frequency the integrator circuit does not have frequency instability problem as faced in ideal differentiator circuit.

However at low frequency (for dc signal $f=0$) the gain becomes ∞ (saturates) to the solution to this problem is connecting feedback resistor parallel to C_f .

practical / Lossy Integrator:



The gain of an integrator at low frequency (dc) signal) can be limited to avoid the saturation problem if the feedback capacitor is shunted by resistance R_f .

The parallel combination of R_f & C_f behaves like a practical capacitor which dissipates power unlike a ideal capacitor. For this reason this ckt is also called lossy integrator.

$$\frac{V_o(s)}{V_{in}(s)} = \frac{\left(\frac{R_f \cdot s C_f}{R_f + \frac{1}{s C_f}} \right)}{R_i}$$

$$= \frac{\left(-\frac{R_f}{R_i s C_f} \right)}{R_f s C_f + 1}$$

$$= \frac{-\left(\frac{R_f}{R_i} \right)}{1 + s C_f R_f}$$

$$\text{put } s = j\omega$$

$$A = \frac{-\left(\frac{R_f}{R_i} \right)}{1 + j\omega R_f C_f}$$

$$= \frac{-\left(\frac{R_f}{R_i} \right)}{1 + j 2\pi f R_f C_f}$$

$$A = \frac{-\left(\frac{R_f}{R_i} \right)}{1 + j \frac{f}{f_a}}$$

$$\text{where } f_a = \frac{1}{2\pi R_f C_f}$$

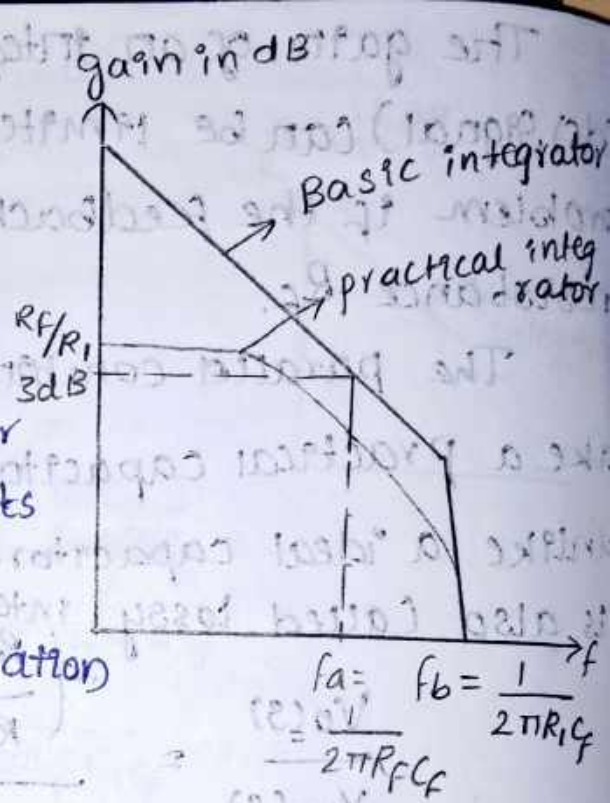
$$|A| = \frac{\left(\frac{R_f}{R_i} \right)}{\sqrt{1 + \left(\frac{f}{f_a} \right)^2}}$$

$$1) f < f_a \Rightarrow A = \frac{-R_f}{R_i}$$

$$2) f = f_a \Rightarrow A = \frac{R_f}{R_i \sqrt{2}}$$

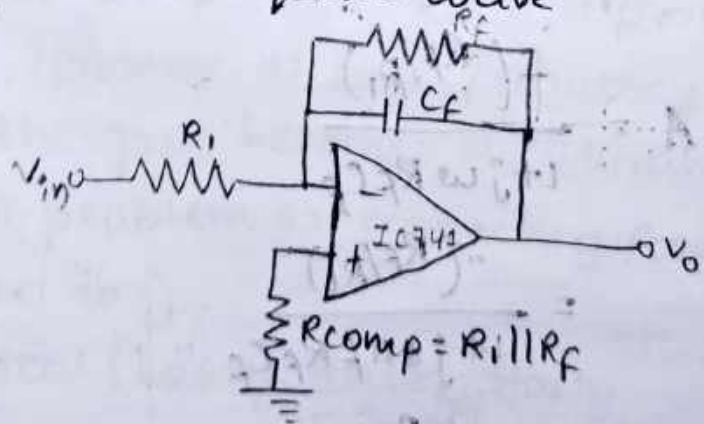
3) $f > f_a \Rightarrow A$ decreases

If the input frequency lower than f_a the circuit acts like a simple inverting amplifier and no integration results.



Consider the lossy integrator. For the component values $R_i = 10k\Omega$, $R_f = 100k\Omega$ & $C_f = 10nF$. Determine the low frequency limit of integration and draw the response for the inputs

- Sine wave $1V_p$, $1kHz$
- Step input $V_i = 1V$ for $0 \leq t < 0.3msec$
- $1V_p$ $5kHz$ Square wave



$$R_i = 10k\Omega$$

$$R_f = 100k\Omega$$

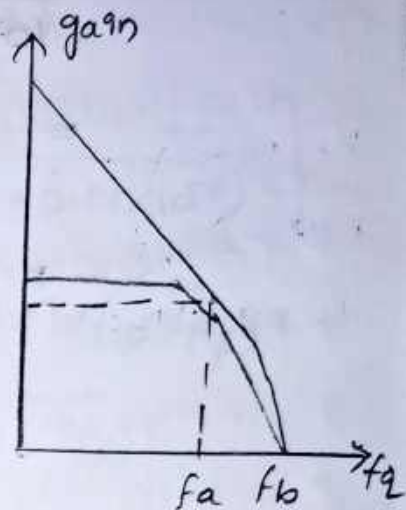
$$C_f = 10nF$$

Low frequency limit of the integrator

$$f_a = \frac{1}{2\pi R_f C_f}$$

$$= \frac{1}{2\pi \times 100 \times 10^3 \times 10 \times 10^{-9}}$$

$$f_a = 159.15 \text{ Hz}$$



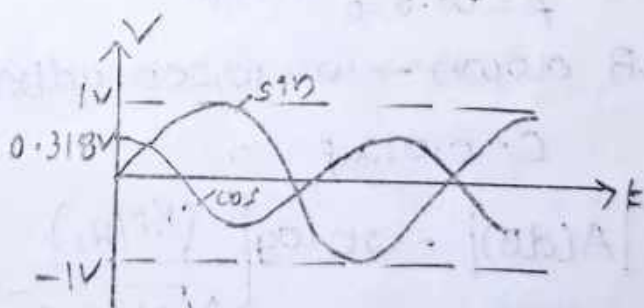
a) $V_{in} = V_p \sin \omega t$
 $= 1 \sin 2\pi f t$

$$V_o = \frac{-1}{R_f C_f} \int V_i dt$$

$$= \frac{-1}{10 \times 10^3 \times 10 \times 10^{-9}} \int \sin 2\pi \times 5 \times 10^3 t$$

$$V_o = \frac{1}{10^{-4}} \left[\frac{\cos 2\pi 5000 t}{2\pi 5000} \right]$$

$$= 0.318 \cos(2\pi 5000 t)$$

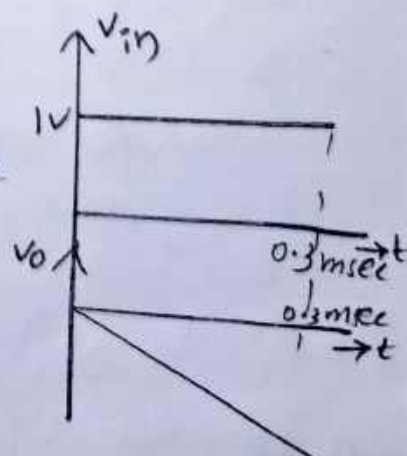


b) $V_o = \frac{-1}{R_f C_f} \int V_i dt$

$$= \frac{-1}{10 \times 10^3 \times 10 \times 10^{-9}} \int_0^{0.3 \text{ msec}} 1 dt$$

$$= \frac{1}{10^{-4}} [t]_0^{0.3 \text{ msec}}$$

$$= \frac{0.3 \times 10^{-3}}{10^{-4}} = -3V$$



$$\begin{aligned}
 c) \quad V_o &= \frac{-1}{R_f C_f} \int v_i dt & f &= 5 \text{ KHz} \\
 &= \frac{-1}{10^{-4}} \int_0^{0.1 \text{ msec}} 1 dt & t &= \frac{1}{5 \times 10^3} = 0.2 \text{ msec} \\
 &= \frac{-1}{10^{-4}} [t]_0^{0.1 \text{ msec}} \\
 &= \frac{-1}{10^{-4}} \times 0.1 \times 10^{-3} \\
 &= -1 \text{ V}
 \end{aligned}$$

Find R_i & R_f in lossy integrator so that the peak gain is 20dB and a gain is 3dB down from the peak when $\omega = 10,000 \text{ rad/sec}$ use a capacitance of $0.01 \mu\text{F}$.

peak gain is 20dB
 $f = \omega \cdot 0 = 0$

3dB down $\rightarrow \omega = 10,000 \text{ rad/sec}$

$C = 0.01 \mu\text{F}$

$$|A(\text{dB})| = 20 \log \left[\frac{(R_f/R_i)}{\sqrt{1 + (\omega R_f C_f)^2}} \right]$$

$$20 = 20 \log \left[\frac{(R_f/R_i)}{\sqrt{1 + 0}} \right]$$

$$1 = \log \left(\frac{R_f}{R_i} \right)$$

$$\frac{R_f}{R_i} = 10$$

$$R_i = \frac{R_f}{10}$$

At $\omega = 10^4 \text{ rad/sec}$

$$17 = 20 \text{ dB} \log \left[\frac{R_f/R_i}{\sqrt{1 + (\omega R_f C_f)^2}} \right]$$

$$17 = 20 \log \left[\frac{10}{\sqrt{1 + (10^4 \times R_f \times 0.01 \times 10^{-6})^2}} \right]$$

$$17 = 20 \log_{10} 10 - 20 \log \sqrt{1 + (10^{-4} R_f)^2}$$

$$17 = 20 - 20 \log \sqrt{1 + (10^{-4} R_f)^2}$$

$$20 \log \sqrt{1 + (10^{-4} R_f)^2} = 20 - 17$$

$$20 \times \frac{1}{2} \log [1 + (10^{-4} R_f)^2] = 3$$

$$\log [1 + (10^{-4} R_f)^2] = \frac{3}{10}$$

$$[1 + (10^{-4} R_f)^2] = 10^{3/10}$$

$$[1 + (10^{-4} R_f)^2] = 2$$

$$[10^{-4} R_f]^2 = 2 - 1$$

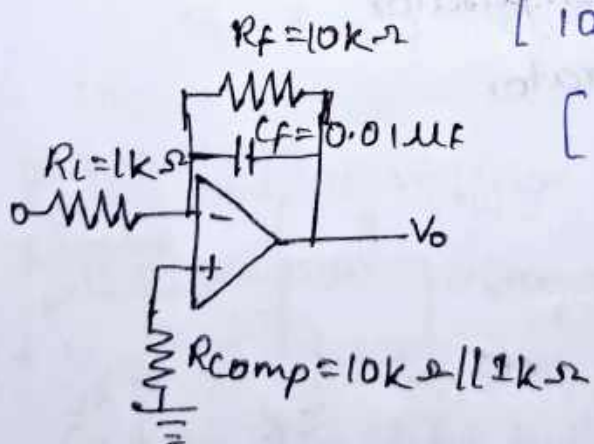
$$[10^{-4} R_f]^2 = 1$$

$$10^{-4} R_f = 1$$

$$R_f = \frac{1}{10^{-4}}$$

$$R_f = 10^4$$

$$R_f = 10 \text{ k}\Omega$$



$$\frac{R_f}{R_i} = 10 \quad (1)$$

$$R_i = \frac{R_f}{10} = \frac{10 \text{ k}\Omega}{10} = 1 \text{ k}\Omega$$

An Op-Amp in open loop configuration operates in a non-linear manner. There are no applications of op-amp in this mode. They are:-

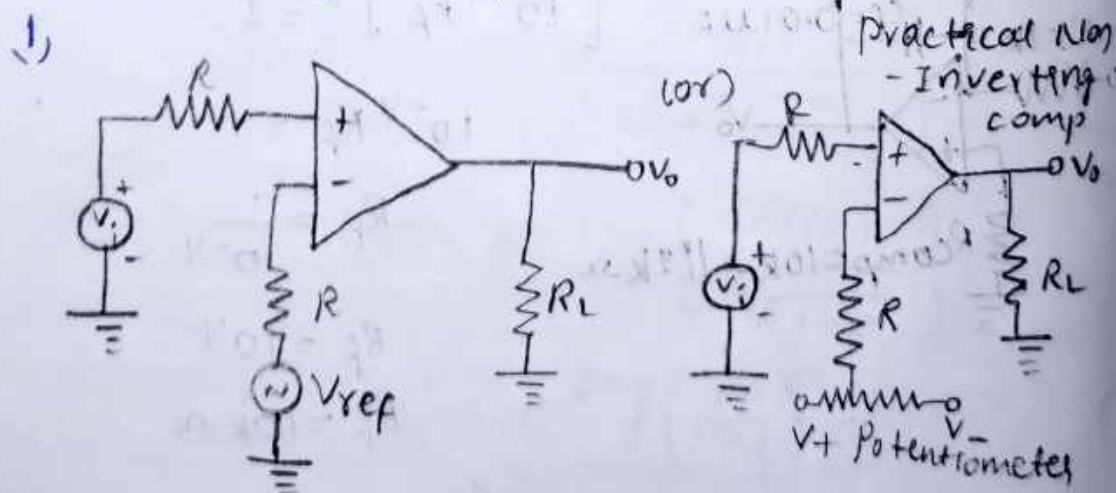
- * Comparator
- * Detector
- * Limiter
- * Digital Interfacing device [converters]

Comparator:-

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other end.

Types of Comparators:-

- 1) Non-Inverting Comparator
- 2) Inverting comparator

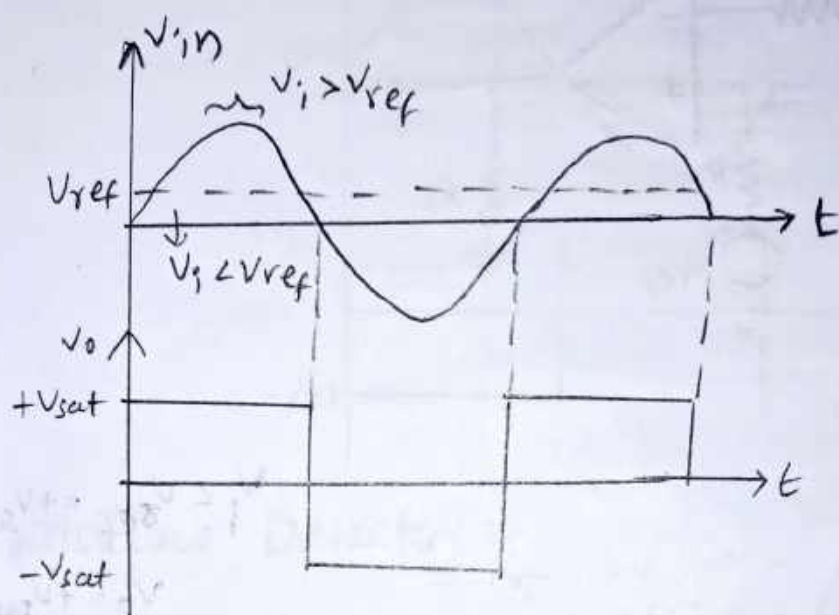


① $V_+ > V_- \Rightarrow V_o = +V_{sat}$

② $V_+ < V_- \Rightarrow V_o = -V_{sat}$

$$\textcircled{1} V_{in} < V_{sat} \Rightarrow V_o = -V_{sat}$$

$$\textcircled{2} V_{in} > V_{sat} \Rightarrow V_o = +V_{sat}$$



* A fixed reference V_{ref} voltage is applied to the -ve input terminal and time varying signal V_i is applied at the positive input terminal. Here the Op-amp we are operating in open-loop configuration.

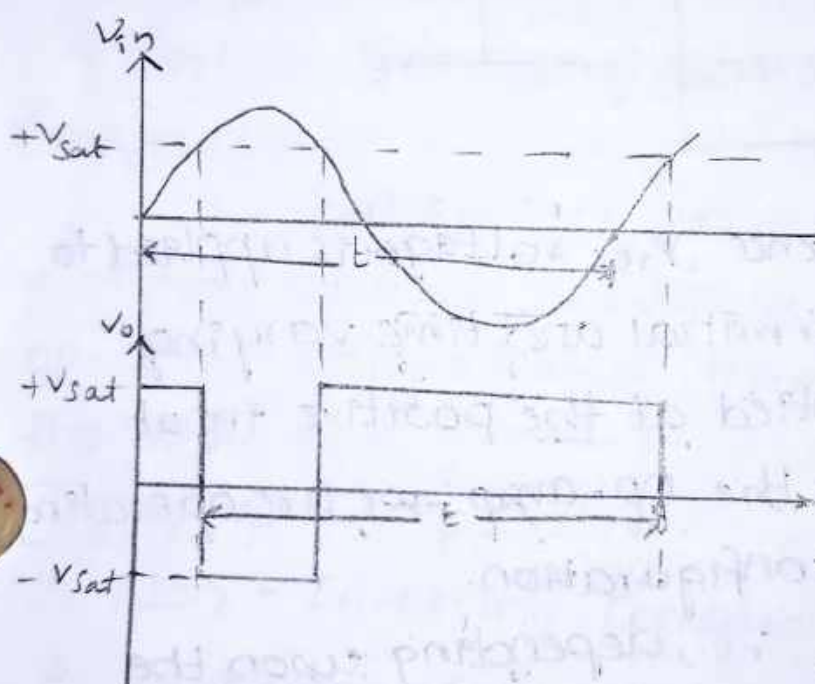
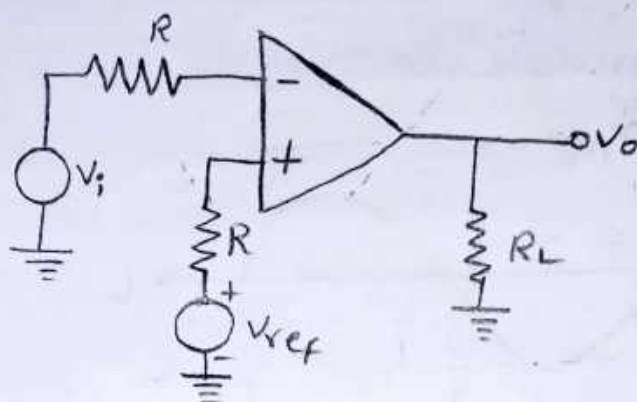
$V_o = \pm V_{sat}$ i.e., depending upon the input voltage.

* The output voltage $V_o = -V_{sat}$ for $V_i < V_{ref}$.

* The output voltage $V_o = +V_{sat}$ for $V_i > V_{ref}$.

* V_{ref} of desired amplitude and polarity can be obtained by simply adjusting the $10k\Omega$ potentiometer.

2, Inverting Comparator



$$V_i < V_{ref} \Rightarrow +V_{sat}$$

$$V_o = +V_{sat}$$

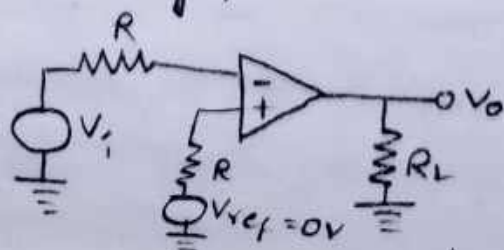
Applications of Comparator:-

Zero Crossing detector

Window detector

Time marker generator etc

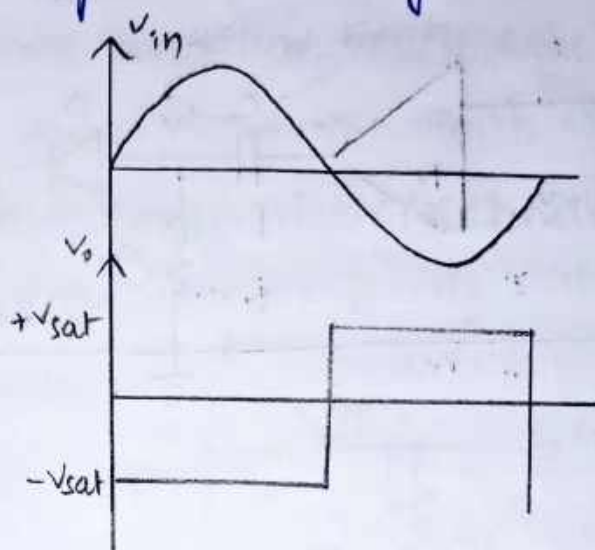
1) Zero Crossing detector:-



$$V_i > V_{ref}$$

$$V_o = -V_{sat}$$

The basic comparator can be used as a zero crossing detector by connecting $V_{ref} = 0V$.



Window Detector :-

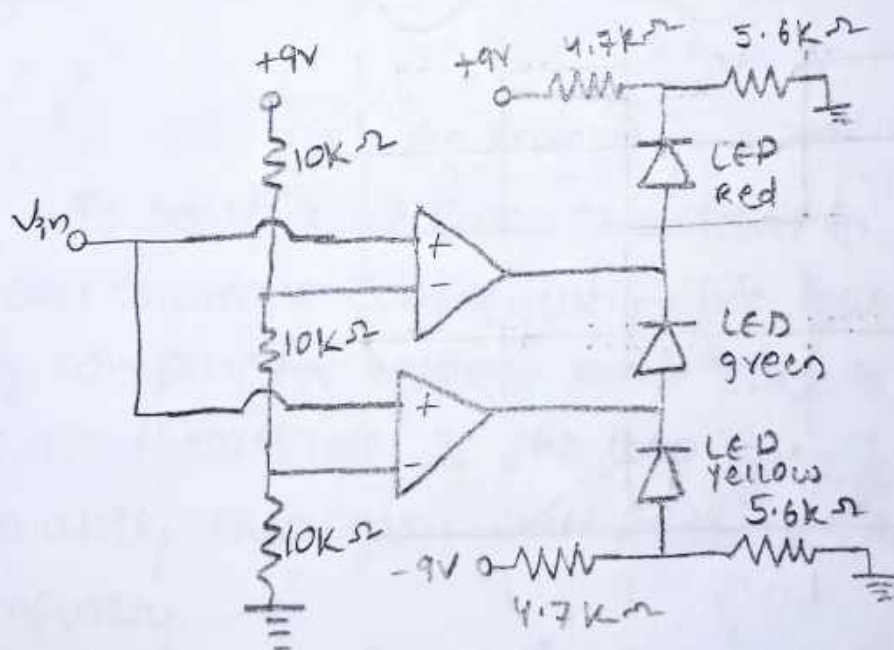
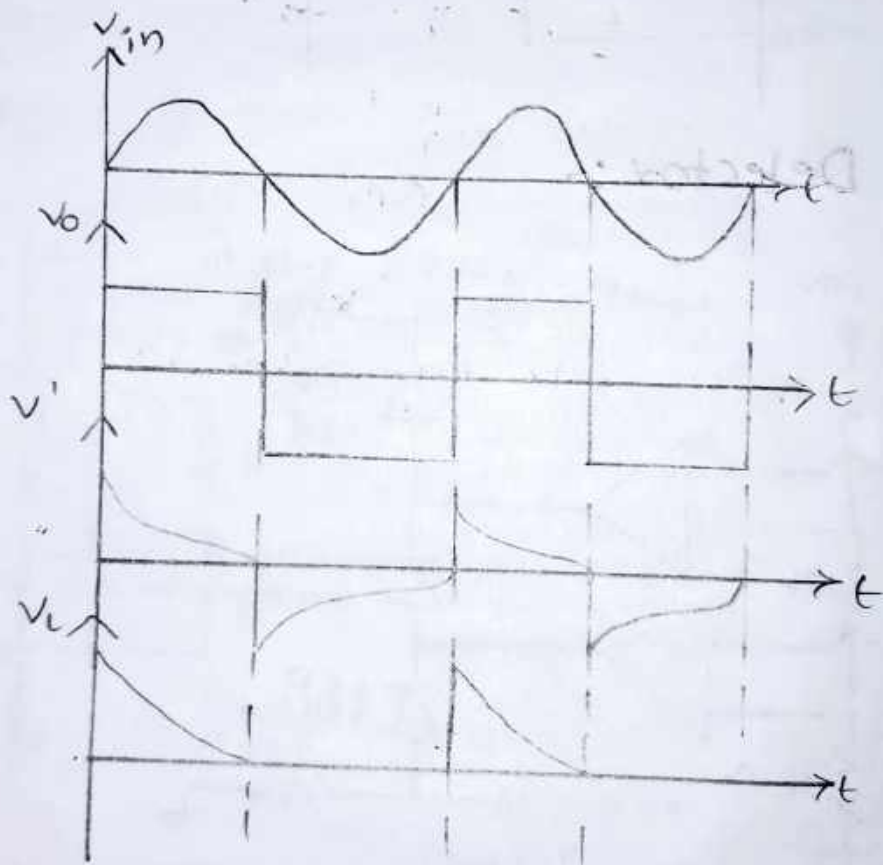
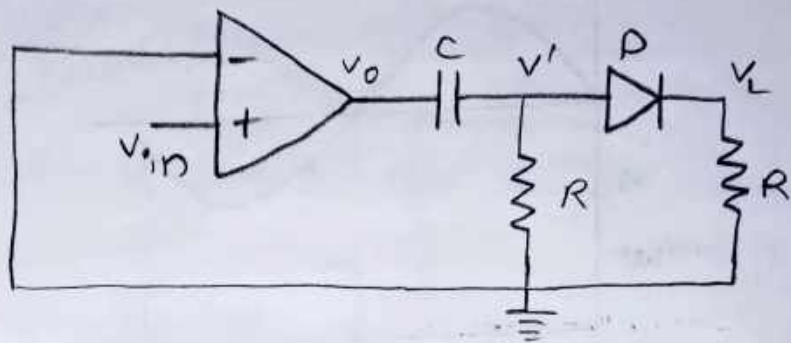


Fig:- 3 level comparator with LED indicators

Input	LED ₃	LED ₂	LED ₁
$V_i < 3V$	ON	OFF	OFF
$3V < V_i < 6V$	OFF	ON	OFF
$V_i > 6V$	OFF	OFF	ON

Time Marker generator



The output of zero crossing detector is differentiated by an RC circuit ($R_C \ll T$). So with the help of this So that the voltage v' is a series of positive and negative pulses as shown in figure. The diode will allow only positive pulses and negative pulses are clipped off that we are observing as load voltage in the waveform.

This triggering pulses are used in monostable multivibrator, Astable multivibrator, SCR (Silicon Controlled Rectifier), Sweep voltage of CRT.

Regenerative comparator (Schmitt Trigger)

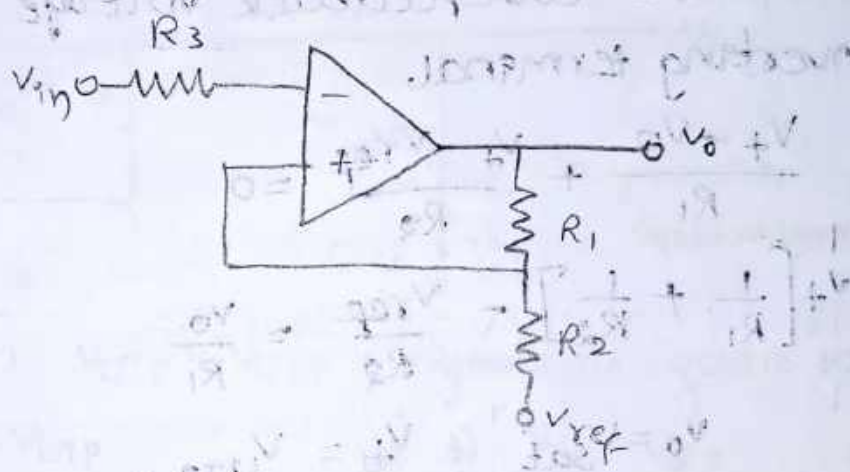


Fig:- An Inverting Schmitt Trigger

If positive feedback is added to the ^{comparator} gain ^{ckt} can increase consequently. The transfer curve of comparator becomes more close to ideal curve, theoretically if the loop gain is adjusted to unity then gain with feedback (A_{CL}) becomes infinity.

$$A_{CL} = \frac{A}{1 - A\beta}$$

$$\text{If } A\beta = 1$$

$$\frac{A}{1-1} = \frac{A}{0} = \infty$$

This results in an abrupt transition between extreme values of the output voltage. In practical circuit however it may not be

possible to maintain loop gain exactly equal to unity ($AB=1$) for a long time because of supply voltages & temperature variations. So a value greater than unity chosen.

→ In a circuit the V_i is applied to the inverting input terminal and feedback voltage to the non-inverting terminal.

$$\frac{V_i - V_o}{R_1} + \frac{V_i - V_{ref}}{R_2} = 0$$

$$V_i \left[\frac{1}{R_1} + \frac{1}{R_2} \right] - \frac{V_{ref}}{R_2} = \frac{V_o}{R_1}$$

$$V_o = V_{sat} \quad V_i = V_{UTP}$$

$$V_{UTP} \left[\frac{1}{R_1} + \frac{1}{R_2} \right] = \frac{V_{ref}}{R_2} + \frac{V_{sat}}{R_1}$$

$$V_{UTP} \left[\frac{R_2 + R_1}{R_1 R_2} \right] = \frac{V_{sat}}{R_1} + \frac{V_{ref}}{R_2}$$

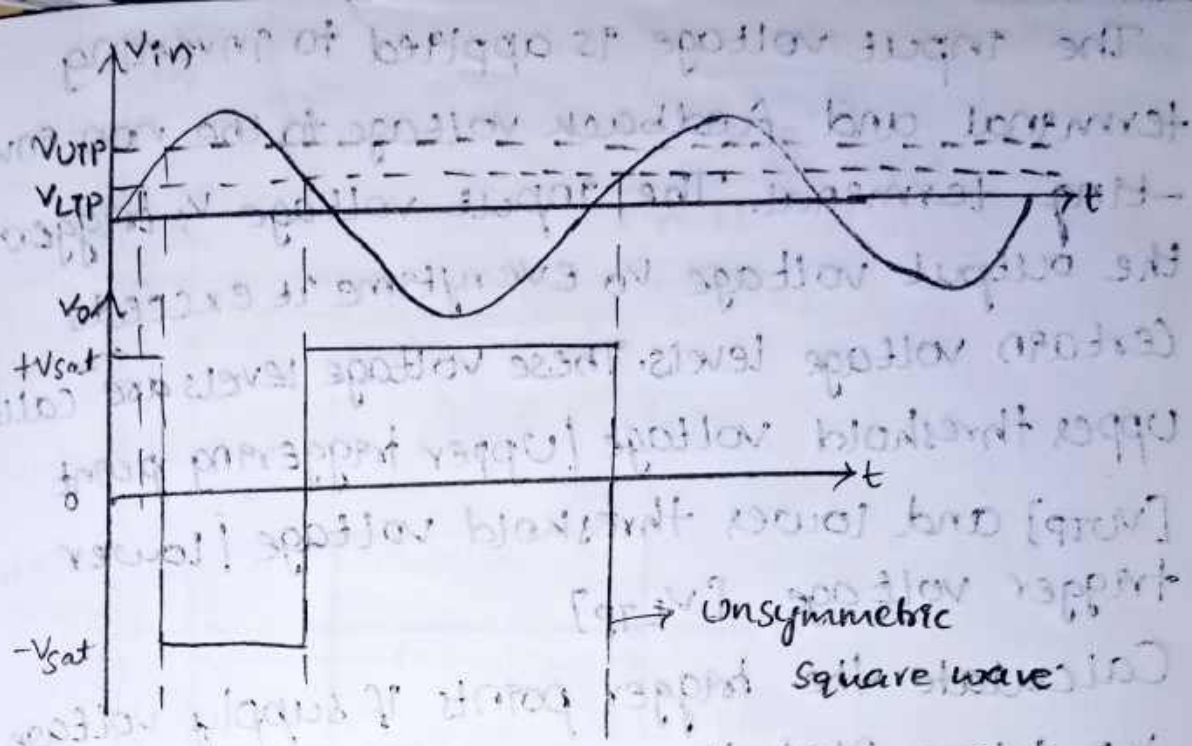
$$V_{UTP} = \left(\frac{R_2}{R_2 + R_1} \right) V_{sat} + \left(\frac{R_1}{R_1 + R_2} \right) V_{ref}$$

Similarly

$$V_{LTP} = - \left(\frac{R_2}{R_2 + R_1} \right) V_{sat} + \left(\frac{R_1}{R_1 + R_2} \right) V_{ref}$$

$$V_{HL} = V_{UTP} - V_{LTP}$$

$$= 2V_{sat} \left(\frac{R_2}{R_1 + R_2} \right)$$



① When $V_{UTP} = V_{LTP} \Rightarrow$ Symmetric Square wave

② $V_i < V_{LTP}$

$$V_- < V_+$$

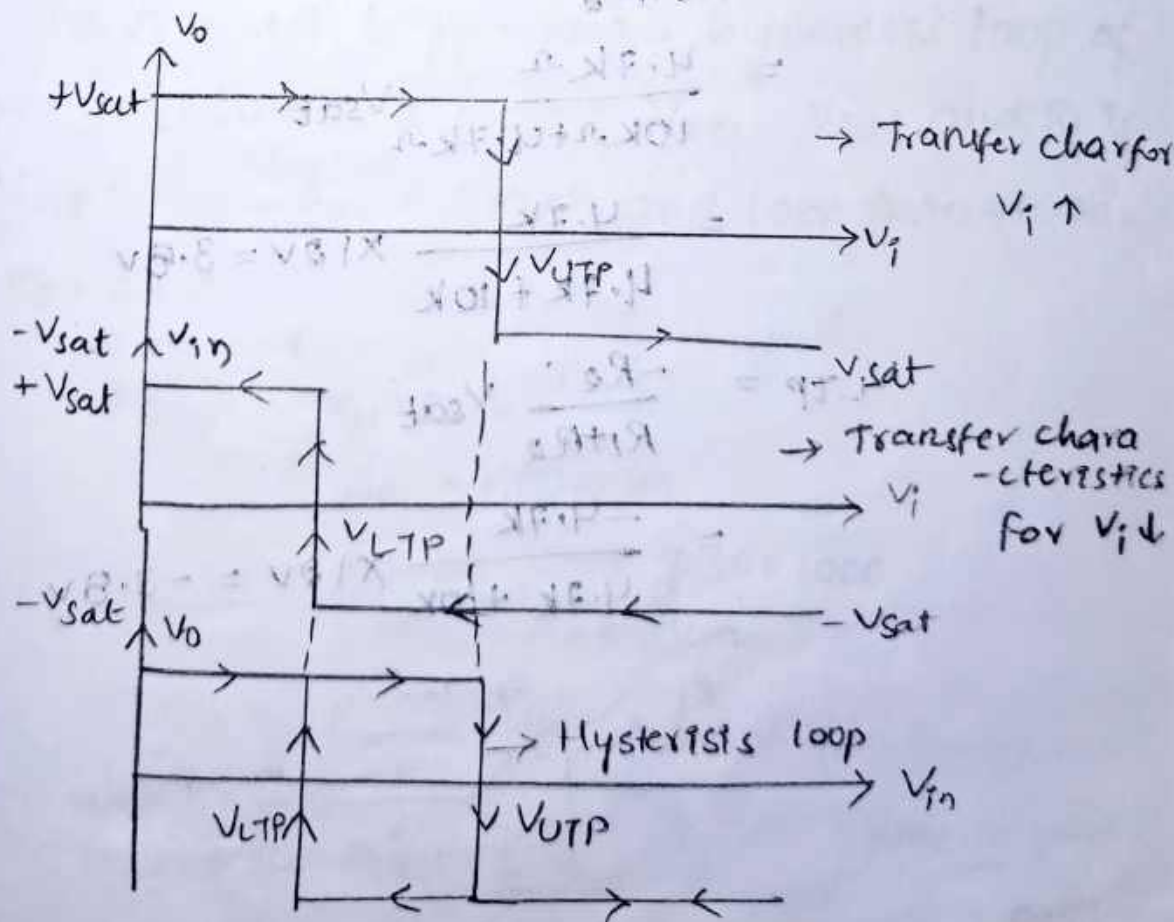
$$V_o = +V_{sat}$$

③ $V_{in} > V_{UTP}$

$$V_- > V_+$$

$$V_{UTP} = V_+$$

$$V_- > V_+ \Rightarrow V_o = -V_{sat}$$

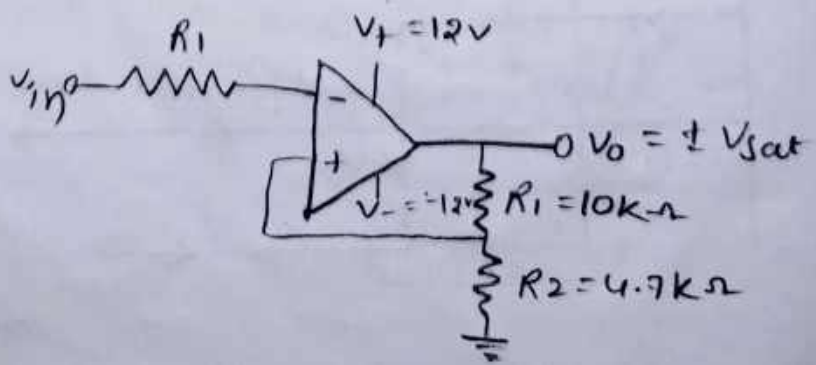


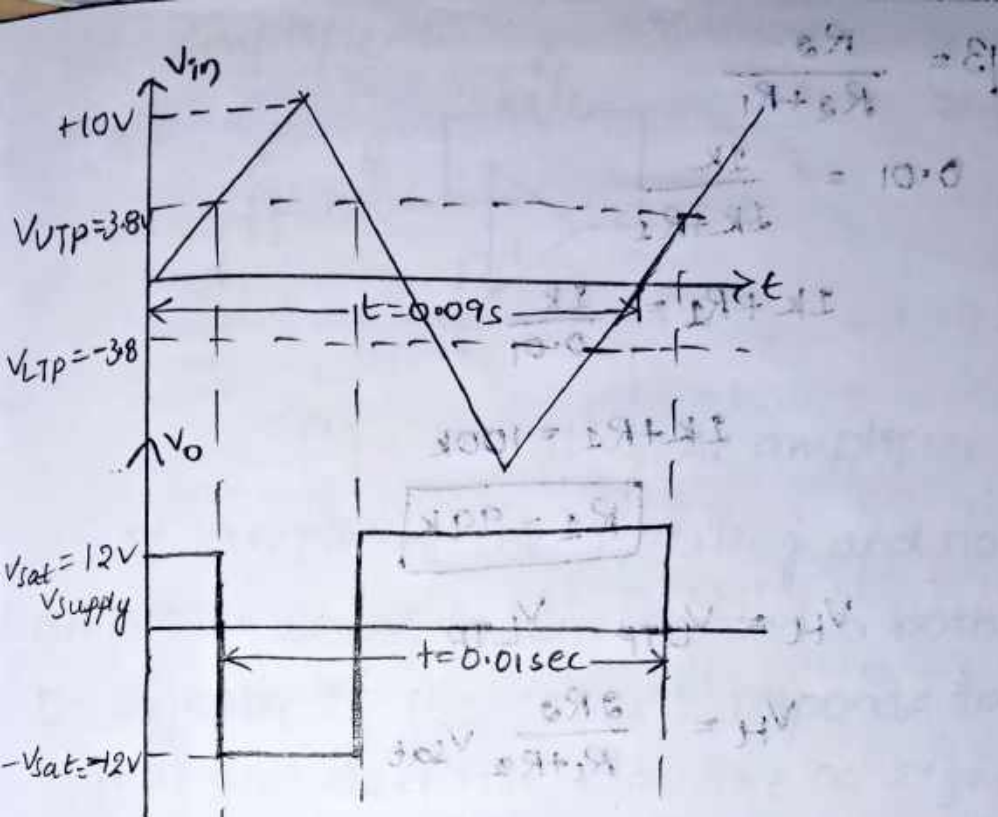
The input voltage is applied to inverting terminal and feedback voltage to the non-inverting terminal. The input voltage V_i triggers the output voltage V_o everytime it exceeds certain voltage levels. These voltage levels are called upper threshold voltage [upper triggering point $[V_{UTP}]$ and lower threshold voltage [lower trigger voltage $[V_{LTP}]$

Calculate the trigger points if supply voltage $V = \pm 12V$. Plot the output voltage $V_o(t)$ if V_i is a 100Hz triangular wave of magnitude $\pm 10V$ ($R_1 = 10k\Omega$, $R_2 = 4.7k\Omega$)

$$\begin{aligned}
 V_{UTP} &= \frac{+R_2}{R_1 + R_2} V_{sat} \\
 &= \frac{4.7k\Omega}{10k\Omega + 4.7k\Omega} V_{sat} \\
 &= \frac{4.7k}{4.7k + 10k} \times 12V = 3.8V
 \end{aligned}$$

$$\begin{aligned}
 V_{LTP} &= \frac{-R_2}{R_1 + R_2} V_{sat} \\
 &= \frac{-4.7k}{4.7k + 10k} \times 12V = -3.8V
 \end{aligned}$$





① $V_{UTP} > V_{in} \Rightarrow V_o = +V_{sat}$

② $V_{LT} < V_{in} \Rightarrow V_o = -V_{sat}$

The Schmitt trigger has a hysteresis loop of $0.1V$ is desired. Calculate V_{ref} , V_{sat} and R_1 if $V_{UTP} = V_{ref}$, $A_{OL} = 1 \text{ lakh}$ and loop gain $= 1000$, $R_2 = 1k\Omega$

$$V_H = 0.1V$$

$$A_{OL} = 1,00,000$$

$$A_{OL}\beta = \text{loop gain} = 1000$$

$$R_2 = 1k\Omega$$

$$V_{sat} = ? , V_{ref} = ?$$

$$R_1, V_{UTP} = V_{sat}$$

$$\beta = \frac{A_{OL}\beta}{A_{OL}} = \frac{1000}{100000} = 0.01$$

$$\beta = \frac{R_2}{R_2 + R_1}$$

$$0.01 = \frac{1k}{1k + R_1}$$

$$1k + R_1 = \frac{1k}{0.01}$$

$$1k + R_1 = 100k$$

$$\boxed{R_1 = 99k}$$

$$V_H = V_{UTP} - V_{LTP}$$

$$V_H = \frac{2R_2}{R_1 + R_2} V_{sat}$$

$$0.1 = \frac{2 \times 1k}{1k + 99k} \times V_{sat} \quad (1)$$

$$0.1 = \frac{2k}{100k} V_{sat} \quad (2)$$

$$0.1 = \frac{2}{100} V_{sat}$$

$$10 = 2 V_{sat}$$

$$\boxed{V_{sat} = 5V}$$

$$V_{UTP} = \frac{R_2}{R_1 + R_2} V_{sat} + \frac{R_1}{R_1 + R_2} V_{ref}$$

$$V_{UTP} = V_{ref}$$

$$V_{ref} \left[1 - \frac{R_1}{R_1 + R_2} \right] = \frac{R_2}{R_1 + R_2} V_{sat}$$

$$V_{ref} \left[\frac{R_2}{R_1 + R_2} \right] = \left[\frac{R_2}{R_1 + R_2} \right] V_{sat}$$

$$\boxed{V_{ref} = V_{sat} = 5V}$$

AC Amplifier:-

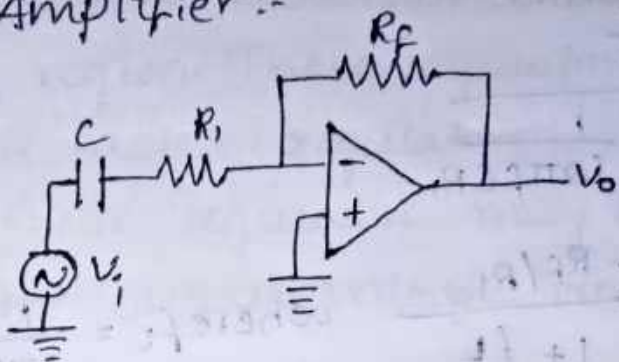


Fig:- Inverting AC amplifier

AC amplifier the inverting and non-inverting amplifier configurations respond to both AC and DC signals. If the circuit responds to only AC signal and does not allow the DC signal for this to block the DC component we are connecting coupling capacitor (C) at the input side of the inverting amplifier.

The Capacitor C blocks the DC component of the input together the resistor (R_i) sets the lower 3dB frequency of the amplifier.

$$V_o = -\frac{R_f}{R_i} V_i$$

$$V_o(s) = \frac{-R_f}{R_i + \frac{1}{sC}} V_i(s)$$

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_f}{R_i \left(1 + \frac{1}{sCR_i}\right)}$$

$$= \frac{-R_f/R_i}{\left(1 + \frac{1}{j\omega CR_i}\right)}$$

$$= \frac{-\frac{R_f}{R_1}}{1 + \frac{1}{j2\pi f C R_1}}$$

$$= \frac{-R_f/R_1}{1 + \frac{f_L}{jf}} \quad \text{where } f_L = \frac{1}{2\pi R_1 C}$$

In the mid band range of frequency the capacitor C behaves as the short circuit. Therefore the equation becomes,

$$A_{CL} = -\frac{R_f}{R_1}$$

Voltage Regulators:-

The function of voltage regulator is to provide a stable DC voltage for powering the other electronic circuits.

A voltage regulator should be capable of providing substantial output current.

Voltage regulators are classified as

i) Series Regulator [Linear]

ii) Shunt Regulator [Switching]

Series Voltage Regulator:-

In this Regulators, the power transistors are connected in series with between the unregulated DC input and output. The output voltage is controlled by continuous voltage drop across the series pass transistor.

Since, the transistor conductive in active (or) linear region. These regulators are also called linear active regulators.

Linear regulators may have fixed (or) variable output voltage and could be positive or negative.

* 78xx positive voltage Regulator

* 79xx Negative voltage Regulator.

Switching Regulator:-

In this power transistor operates as a high frequency ON/OFF switch. So that power transistor does not conduct current continuously. This gives improved efficiency over the series voltage regulator.

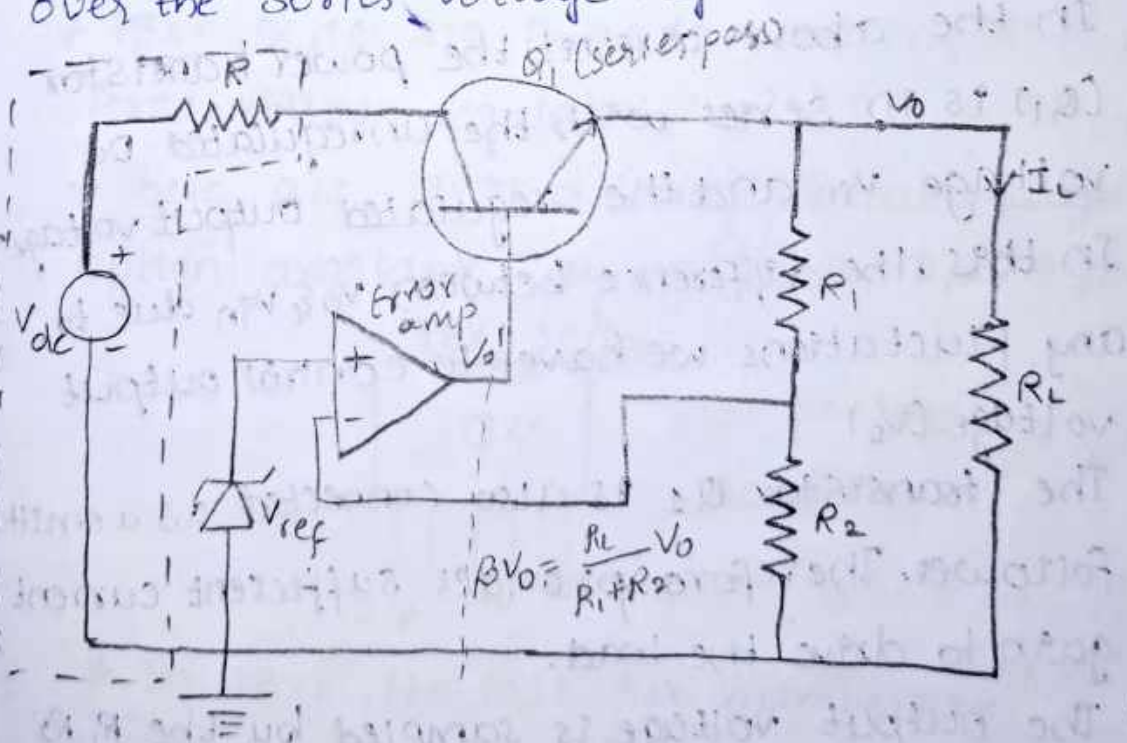


Fig:- Series Regulator (or) Linear (or) Active Regulator

- * A Voltage regulator is an electronic circuit that provides a (DC) stable DC voltage independent of the load current, temperature, AC line voltage regulators. variations
- * Figure shows the regulated power supply using discrete Components.
- * The circuit consists of four parts:-
 - i) Reference voltage circuit
 - ii) Error amplifier
 - iii) Series pass transistor
 - iv) Feedback Network
- * In the above circuit the power transistor (Q_1) is in series with the unregulated DC voltage V_{in} and the regulated output voltage.
- * In this, the difference between V_o & V_{in} due to any fluctuations we have to control output voltage (V_o).
- * The transistor Q_1 is also connected as a emitter follower. Therefore provides sufficient current gain to drive the load.
- * The output voltage is sampled by the R_1, R_2 divider and the feedback to the inverting terminal of the Op-amp i.e., error amplifier.
- * This sampled voltage is compared with the reference voltage (V_{ref}) (usually obtained by the

zener diode]

- * The output voltage V_o' of the error amplifier drives the series pass transistor Q_1 to work.
- * If the output voltage increases due to the variations in the load current, the sampled voltage PV_o also increases.

If $PV_o > V_{ref}$; $V_o' = \text{Less volts}$

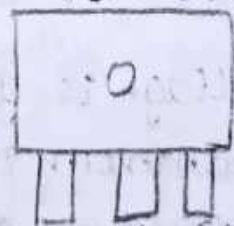
- * The less o/p voltage V_o' is connected to the base of the transistor, the transistor will amplify the less voltage and we observe V_o' is less voltage.

Fixed Series Voltage Regulator [Three terminal Voltage Regulator]

- * 78xx series are three terminal positive fixed voltage regulators.

- * There are seven different output voltage options available. They are 5, 6, 8, 12, 15, 18 & 24V.

78xx series



Flat package

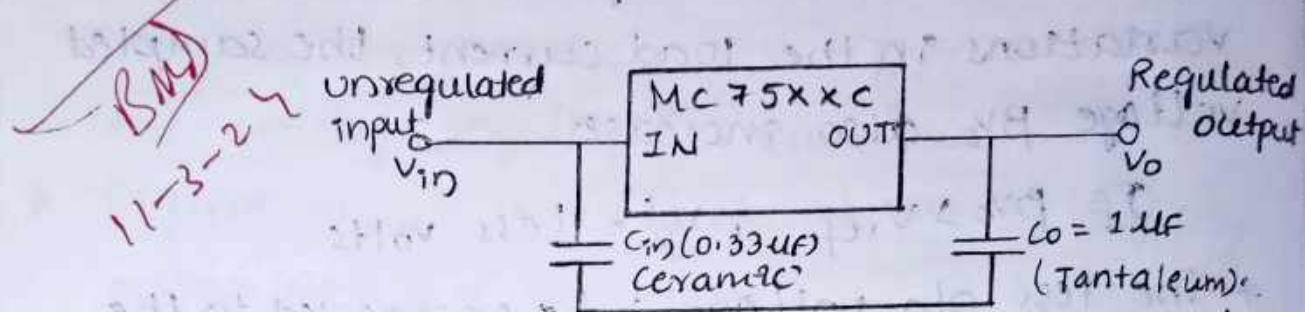
IC 78xx

I/P O/P GND

- * In 78xx, the last two numbers xx indicates the output voltage.

For eg:- 7855 represents a +5V regulator.

Similarly 79xx Series fixed voltage regulators. There are two extra voltage options other than 78xx series. They are $-2V$ & $-5.2V$



Standard representation of three terminal positive monolithic regulator.

→ Input Capacitor C_{in} (0.33 μF) is usually connected between input terminal and ground to cancel the inductive effect due to long distribution leads.

→ The output capacitor C_o (1 μF) improves the transient response.

Characteristics:-

1) V_o :- Regulated output voltage is fixed at a value has specified by the manufacture.

eg:- 7805 has a output voltage of $V_o = 5V$

7912 has a output voltage of $V_o = 12V$

2) $|V_{in}| \geq |V_o| + 1.2V$

For 7805 the input voltage is greater than or equal to 7 volts. For 7912 the minimum ip voltage is $-14V$.

3) $I_o \max$ → load current vary from 0 to rated max output current.

4) Thermal shutdown:- The integrated circuit has temperature sensors (built in) which turns off the IC when it becomes too hot using $125^\circ C$ to $150^\circ C$

5) Line/ Input Regulation:-

It is defined as the percentage change in the output voltage for the change in the input voltage. It is usually expressed in mV for 7805 line.

regulation is 3mV

1) Load Regulation:- $\frac{\Delta V_o}{\Delta V_{in}}$

It is defined as change in the output voltage for change in (input) load current. $\frac{\Delta V_o}{\Delta V_{in}}$

2) Ripple Rejection:-

The IC Regulator not only keeps the output voltage constant but also reduces the amount of ripple voltage it is usually expressed in decibels.

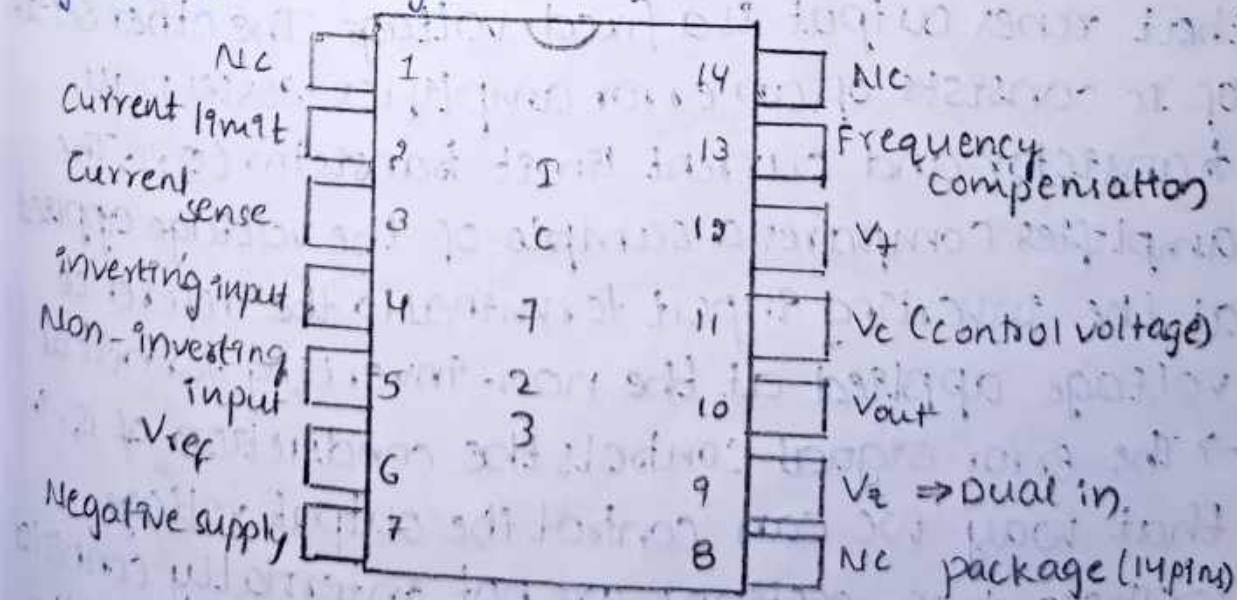
For 7805 the ripple rejection is 78 decibels

IC 723 voltage regulator (General purpose voltage Regulator).

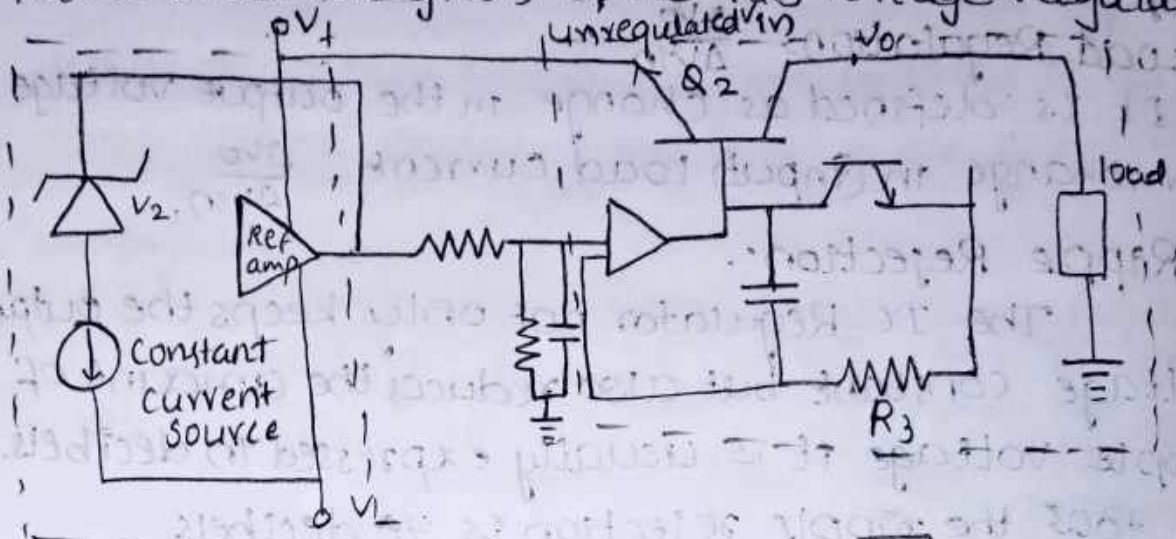
The three terminal voltage regulator have the limitation: 1. No short circuit protection.

2. Output voltage (positive or negative) is fixed.

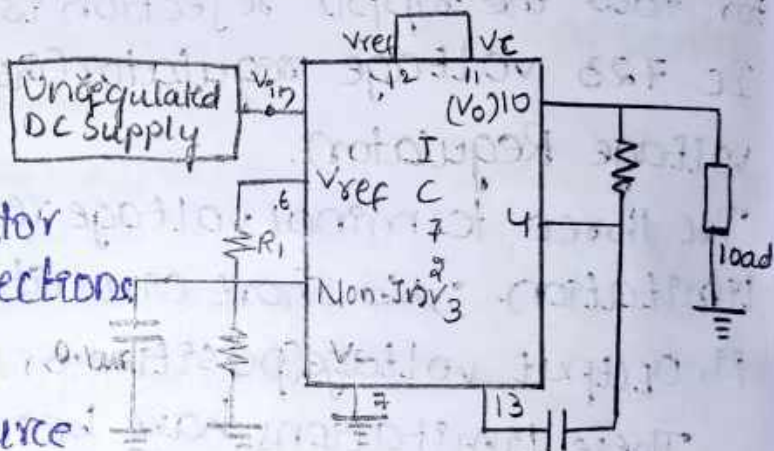
These limitations have been overcome in 723 general purpose regulator which can adjusted over a wide range of both positive and negative regulated voltage.



Functional diagram of IC 723 voltage Regulator



The functional block diagram of 723 voltage regulator IC has 2 separate sections. The zener diode, a constant current source and reference amplifiers produces a fixed voltage of 7 volts at the terminal. The constant current source forces the zener diode to operate at a fixed point so that zener output is a fixed voltage. The other section of IC consists of an error amplifier, series pass transistor and current limit transistor (Q_2). The amplifier compares a sample of the voltage applied at the inverting input terminal to the reference voltage applied at the non-inverting terminal. → The error signal controls the conduction of Q_1 , in that way we can control the output voltage. → These two sections are not internally connected but the various points are brought out on the IC package.



Important features of IC 723

Input voltage is 40V maximum and output voltage is adjustable from 2V to 37V.

Output current 150mA without external pass resistor.

Output current 10Amp is possible by adding external transistor.

It can be used as linear and switching regulator.

By using this IC we can maintain fixed and variable positive & negative voltages.

Internal power dissipation is 800mW.

It has built-in short circuit protection.

The output voltage of the non-inverting terminal $V_{NI} = V_{ref} \frac{R_2}{R_1 + R_2}$

By using error amplifiers we are calculating the difference between V_{NI} and V_o (which is directly feedback to the inverting terminal which amplifies by the error amplifiers).

→ The output of the error amplifiers drives the pass transistor Q_1 so has to minimize the difference between non-inverting and error amplifiers.

→ If the output voltage becomes low the voltage at the inverting terminal of error amplifiers also goes down this makes the output of the error amplifiers to become more positive there by driving the transistor Q_1 more into

the conduction. This reduces the voltage across R_1 and drives maximum current to the load causing voltage across the load to increase. so, the initial drop in the load voltage has been compensated.

→ Similarly any increase in low voltage or change in the input voltage get regulated.

Calculate R_1 & R_2 for a low voltage regulator using 723 IC to get an output voltage of 8V ($V_{ref} = 7V$).

$$V_o = V_{ref} \frac{R_2}{R_1 + R_2}$$

$$3 = 7 \frac{R_2}{R_1 + R_2}$$

$$3R_1 + 3R_2 = 7R_2$$

$$3R_1 = 4R_2$$

$$\text{Assume } R_1 = 10k\Omega$$

$$R_2 = \frac{3}{4} R_1 \Rightarrow \frac{30k}{4} = 7.5k\Omega$$

$$\boxed{R_2 = 7.5k\Omega}$$

UNIT-II

OP-AMP, IC 555 & IC 565

Electronic Filter:-

It is a frequency selective electronic (filter) circuit that passes electric signal of specific band of frequencies and attenuates the signal of frequencies outside the band is called an Electronic Filter.

Types of Filters:-

i) Passive Filter

ii) Active Filter

Passive Filters:-

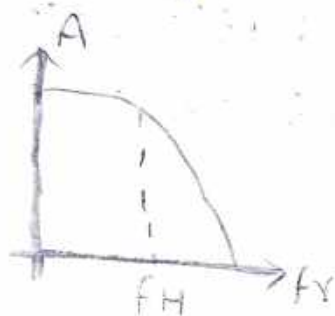
These filters uses passive components (R, L, C). This filters works well for high frequency i.e., Radio frequency.

However, at audio frequency [low freq] inductors become large, heavy and expensive. * For low frequency applications inductor has more number of turns of wire must be used which inturns adds the series resistance due to this inductor performance is degrading and resulting high power dissipation.

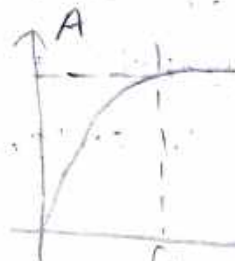
* The active filters overcome the problem of passive filters.

* In this filters Op-amp is a active element resistor & capacitor are the passive elements.

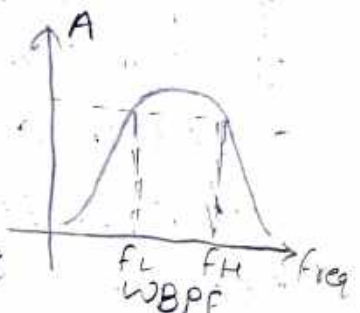
* In the active filters we are operating the op-amp in non-inverting mode [high input impedance, low output impedance] will improve the load drive capacity & the load is isolated from the frequency determining network.



LPF



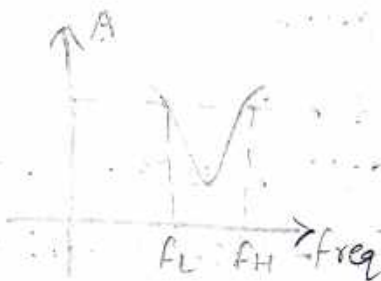
HPF



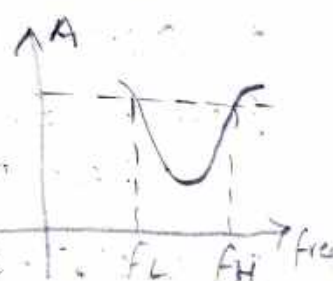
WBPF



NBPF



NBRR



WBRR

Active LPF:-

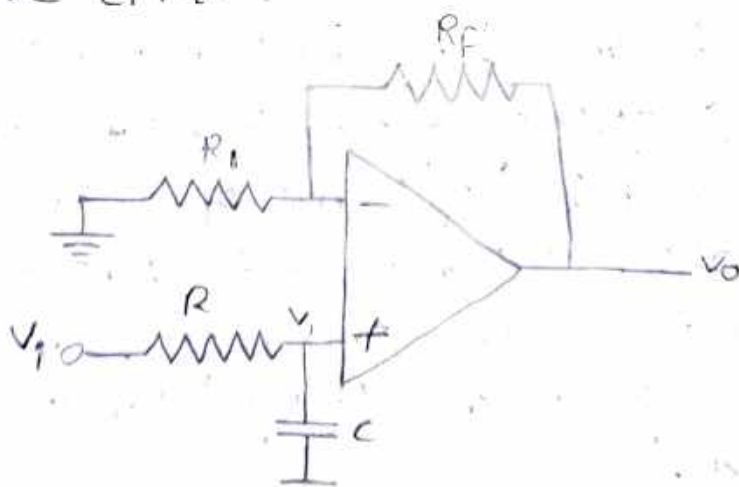


Fig:- First Order Active LPF

$$\frac{V_o(s)}{V_i(s)} = \frac{V_o(s)}{V_i(s)} \times \frac{V_i(s)}{V_i(s)}$$

$$V_i(s) = V_i(s) \frac{\left(\frac{1}{sC}\right)}{\left(\frac{1}{sC} + R\right)}$$

$$\frac{V_i(s)}{V_i(s)} = \frac{\frac{1}{sC}}{\frac{1+sCR}{sC}}$$

$$\frac{V_i(s)}{V_i(s)} = \frac{1}{1+sCR}$$

$$\frac{V_o(s)}{V_i(s)} = A_o$$

$$= \left(1 + \frac{R_f}{R_i}\right)$$

$$\frac{V_o(s)}{V_i(s)} = A_o \left(\frac{1}{1+sCR} \right)$$

put $s = j\omega$

$$\omega = 2\pi f$$

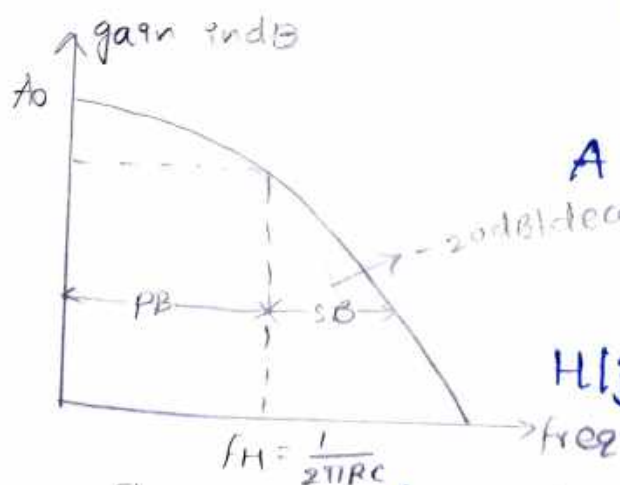
$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{A_o}{1+j\omega RC}$$

$$= \frac{A_o}{1+j2\pi fRC}$$

$$A = \frac{A_o}{1 + \frac{jf}{f_H}}$$

where

$$f_H = \frac{1}{2\pi RC}$$



$$H(j\omega) \text{ (or) } |A| = \frac{A_o}{\sqrt{1 + (f/f_H)^2}}$$

Fig (b):

i) $f < f_H \Rightarrow |A| \approx A_o$

ii) $f = f_H \Rightarrow |A| = \frac{A_o}{\sqrt{2}}$

iii) $f > f_H \Rightarrow |A| = \text{decreases}$

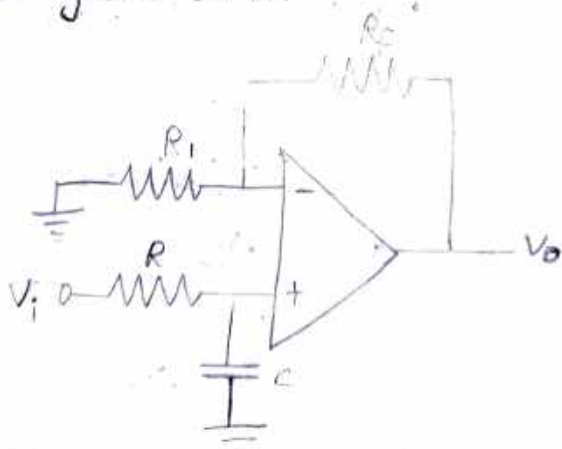
A first order active LPF consists of a single RC network connected to the positive input terminal of the non-inverting op-amp as shown in the figure.

* Resistors R_i and R_f determines the gain of the filter in the pass band.

The frequency response of the first order LPF which is shown in fig (b) has a maximum gain A_0 at frequency 0Hz.

At $f = f_H$ the gain falls to 0.707 times $[-3dB]$ down the maximum gain A_0 .

Design first order LPF with $f_H = 2kHz$ and the pass band gain is 5.



$$f_H = 2kHz$$

$$A_0 = 5$$

$$f_H = \frac{1}{2\pi RC}$$

$$\text{Assume } C = 0.1 \mu F$$

$$R = \frac{1}{2\pi f_C}$$

$$= \frac{1}{2\pi \times 10^3 \times 2 \times 0.1 \times 10^{-6}}$$

$$= 1.5 \text{ k}\Omega$$

$$A_0 = 1 + \frac{R_f}{R_i}$$

$$5 = 1 + \frac{R_f}{R_i}$$

$$\frac{R_f}{R_i} = 4$$

$$\text{Assume } R_i = 1 \text{ k}\Omega$$

$$R_f = 4R_i$$

$$= 4 \times 1 \text{ k}$$

$$R_f = 4 \text{ k}\Omega$$

First Order Active High pass Filter:-

$$\frac{V_o(s)}{V_i(s)} = \frac{V_o(s)}{V_i(s)} \times \frac{V_i(s)}{V_i(s)} \quad - (1)$$

$$V_i(s) = V_i(s) \times \frac{R}{R + \frac{1}{sC}}$$

$$\frac{V_i(s)}{V_i(s)} = \frac{sCR}{sCR + 1} \quad - (2)$$

Substitute eq(2) in eq(1)

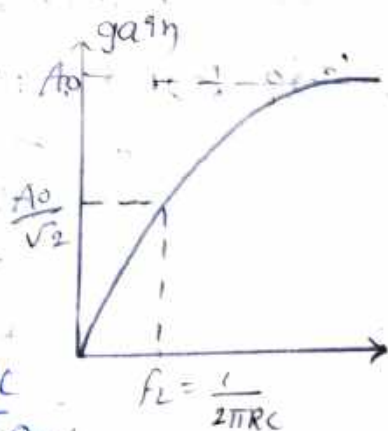
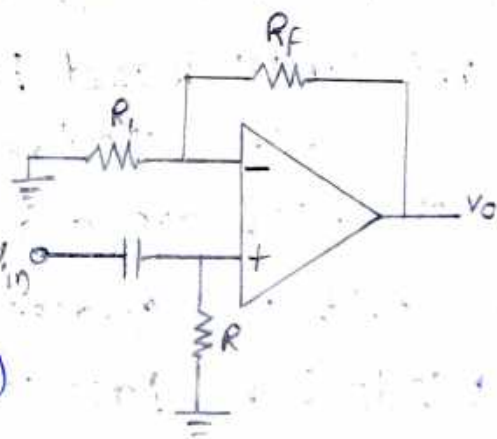
$$\frac{V_o(s)}{V_i(s)} = A_0 \times \frac{sCR}{1 + sCR}$$

$$\text{put } s = j\omega$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = A_0 \frac{j\omega RC}{1 + j\omega RC}$$

$$\text{put } \omega = 2\pi f$$

$$H(j\omega) = A_0 \frac{j2\pi fRC}{1 + j2\pi fRC}$$



put $\omega = 2\pi f$

$$H(f) = \frac{A_0 \frac{jf}{f_L}}{1 + \frac{jf}{f_L}} \quad \text{where } f_L = \frac{1}{2\pi RC}$$

$$|H(j\omega)| = \frac{A_0 \left(\frac{f}{f_L}\right)}{\sqrt{1 + \left(\frac{f}{f_L}\right)^2}}$$

1) $f < f_L \Rightarrow H(j\omega) = \text{gain decreases}$

2) $f = f_L \Rightarrow \frac{A_0}{\sqrt{2}}$

3) $f > f_L \Rightarrow A_0$

Here HPF is the complement of LPF and can be obtained simply by interchanging the resistor and capacitor in the low pass configuration and is shown in figure.

First Order Band Pass Filter:

There are two types of Band pass filters which are classified as per the figure of merit (or) quality factor (Q)

1) Wide band Pass Filter ($Q < 10$)

2) Narrow band Pass Filter ($Q > 10$)

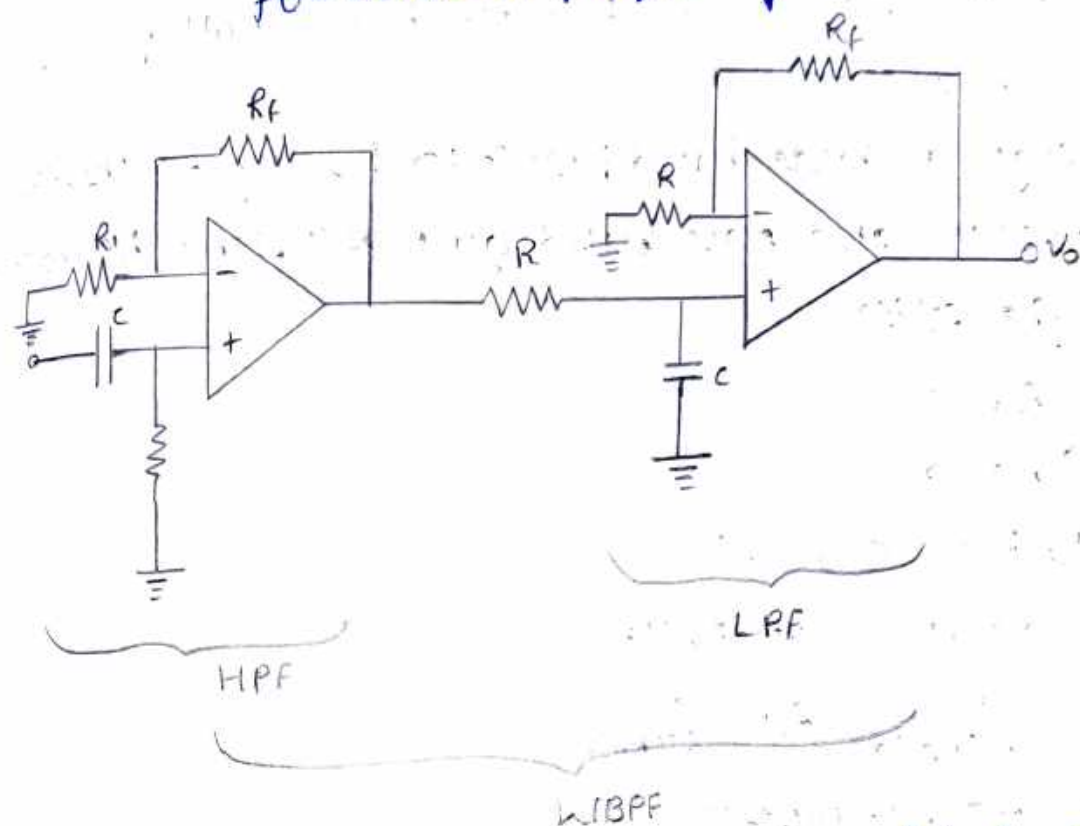
1) Wide Band Pass Filter

$$Q = \frac{f_0}{BW}$$

$$= \frac{f_0}{f_H - f_L}$$

$$f_0 = \sqrt{f_H \cdot f_L}$$

where, f_H = Upper frequency
 f_L = Lower frequency
 f_0 = Centered frequency



A Band Pass Filter has pass band between two cut-off frequencies (f_H and f_L). Any input frequency passes outside pass band is attenuated. Band pass filter can be formed by simply cascading a HPF, LPF sections.

$$H_C(j\omega) = \frac{A_0(f/f_L)}{\sqrt{1 + (f/f_L)^2}}$$

$$H_C(j\omega) = \frac{A_0}{\sqrt{1 + (f/f_H)^2}}$$

$$H_C(j\omega) = \frac{A_{01}(f/f_L)}{\sqrt{1 + (f/f_L)^2}} \times \frac{A_{02}}{\sqrt{1 + (f/f_H)^2}}$$

where $A_{01} \times A_{02} = A_0$

$$H(f) \text{ for BPF is } = \frac{A_0 (f/f_L)}{\sqrt{[1 + (f/f_L)^2 + (1 + f/f_H)^2]}}$$

For the first order BPF we have a roll off rate -20 dB/decade.

Design a wide band pass filter having $f_L = 400\text{Hz}$, $f_H = 2\text{kHz}$ and pass band gain of 4. Find the values of the filter.

$$A_0 = 4$$

$$A_{01} \cdot A_{02} = 4$$

$$A_{01} \approx 2, A_{02} \approx 2$$

$$f_L = 400\text{Hz} \quad f_H = 2\text{kHz}$$

$$f_L = \frac{1}{2\pi R_2 C_2} \quad f_H = \frac{1}{2\pi R_1 C_1}$$

Assume, $C = 0.01\mu\text{F}$

$$R_2 = \frac{1}{2\pi f_L C_2} = \frac{1}{2\pi \times 400 \times 0.01 \times 10^{-6}} = 3.98\text{k}\Omega$$

$$R_1 = \frac{1}{2\pi f_H C_1} = \frac{1}{2\pi \times 2 \times 10^3 \times 0.01 \times 10^{-6}} = 7.9\text{k}\Omega$$

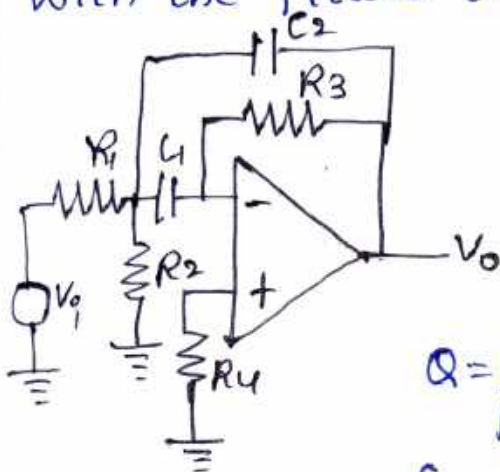
$$Q = \frac{f_0}{\text{BW}} = \frac{f_0}{f_H - f_L} = \frac{\sqrt{f_H - f_L}}{f_H - f_L} = \frac{\sqrt{400 \times 2 \times 10^3}}{2000 - 400}$$

$$Q = 0.56$$

$Q < 10 \rightarrow$ so the filter is WBPF

Narrow Band Pass Filter

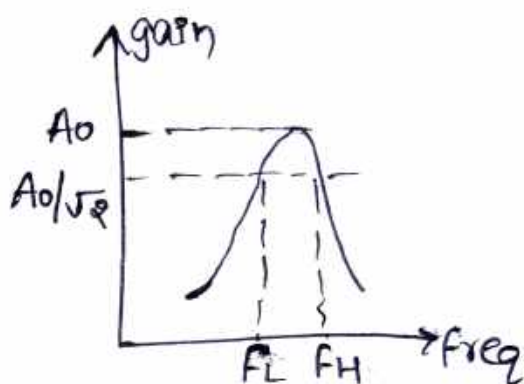
The Narrow BPF is basically a multiple feedback filter. It has a two feedback paths. This filter uses only one op-amp in contrast with the filters [i.e., WBPF]



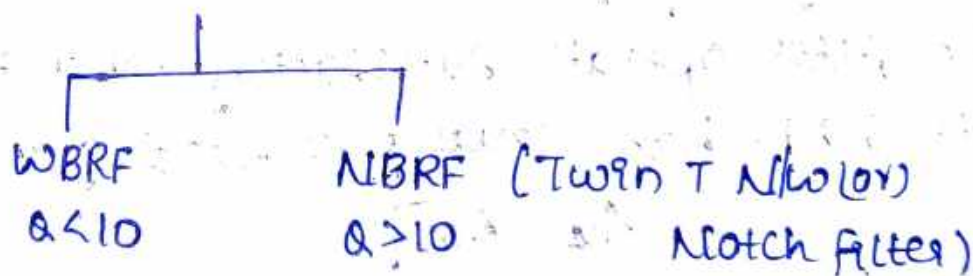
$$Q = \frac{f_c}{BW}$$

$$f_c = \sqrt{f_h - f_l}$$

$$BW = f_h - f_l$$



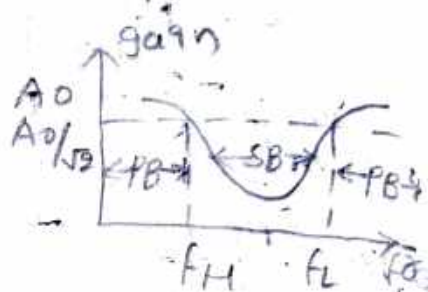
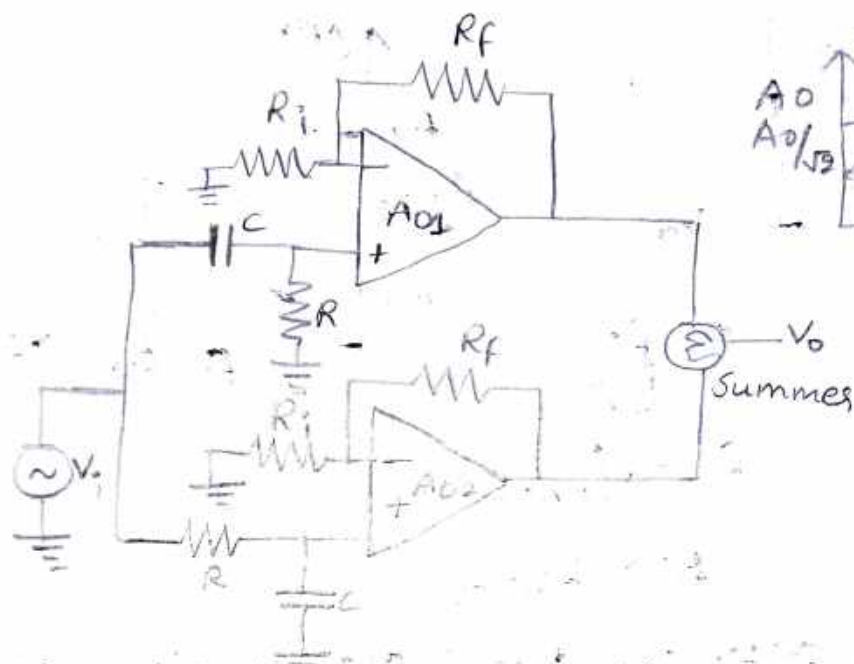
Band Stop Filter (or) Band Eliminating filter
(or) Band Rejection filter



- * The Band stop Filter is also referred as Band rejection (or) Band elimination filters.
- * It has one stop band and two pass bands in their frequency response.

Band Stop Filter attenuates all frequencies between f_L and f_H and transmits ^{all freq} without attenuation below f_L and above f_H . It is opposite to BPF.

WBSF :-



* A WBSF is a combination of LPF, HPF & summing amplifiers.

The filter operates satisfactorily when the LPF & HPF have equal pass band gain

$$A_{01} = A_{02}$$

The lower cut-off frequency f_L of the HPF is greater than the higher cut-off frequency f_H of LPF. $f_L > f_H$

1) Design WBSF having $f_H = 400\text{Hz}$ and $f_L = 2\text{kHz}$ and having pass band gain is '2'.

$$f_H = 400\text{Hz}$$

$$f_L = 2\text{kHz}$$

$$\text{Pass band gain} = 2$$

$$f_n = \frac{1}{2\pi R_1 C_1}$$

(LPF)

Assume $C_1 = 0.1 \mu F$

$$R_1 = \frac{1}{2\pi \times 400 \times 0.1 \times 10^{-6}}$$

$$R_1 = 3.978 k\Omega$$

$$f_L = \frac{1}{2\pi R_2 C_2}$$

(HPF)

Assume $C_2 = 0.1 \mu F$

$$R_2 = \frac{1}{2\pi \times 2 \times 10^3 \times 0.1 \times 10^{-6}}$$

$$R_2 = 795 \Omega$$

pass band gain = $A_{01} = A_{02} = 2$

$$A_{01} = 2$$

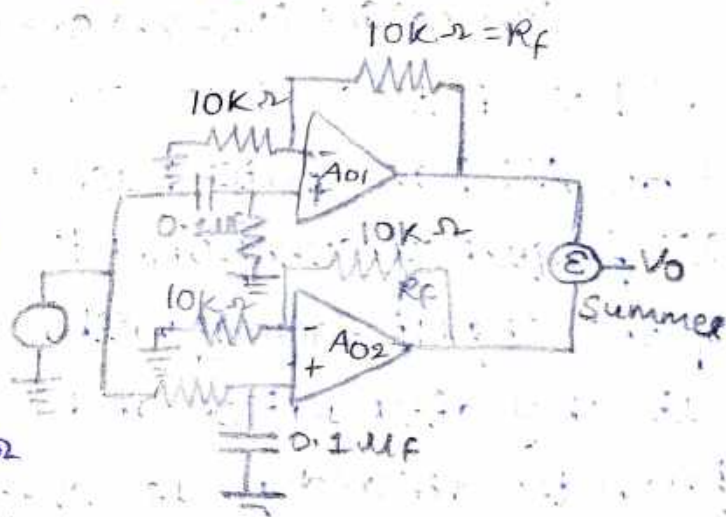
$$1 + \frac{R_f}{R_i} = 2$$

$$\frac{R_f}{R_i} = 1$$

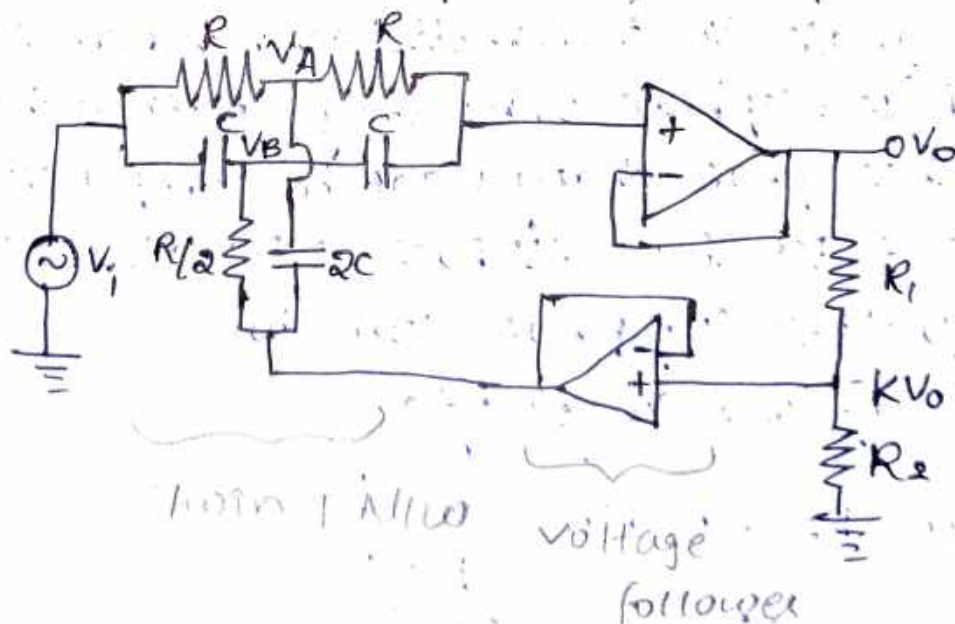
$$R_f = R_i$$

Assume

$$R_f = R_i = 10 k\Omega$$



Narrow Band Stop Filter :- (NBSF)



A Narrow Band Reject Filter commonly called a Notch Filter and is useful for the rejection of single frequency such as ~~50~~ 50Hz power line frequency "Hum".

$$(V_A - V_i)G + (V_A - V_o)G + (V_A - KV_o)2SC = 0$$

$$(V_B - V_i)SC + (V_B - V_o)SC + (V_B - KV_o)2G = 0 \quad (2)$$

$$(V_o - V_A)G + (V_o - V_B)SC = 0 \quad (3)$$

All Pass Filter: (phase corrector / Delay Equalizer):

⇒ An All Pass Filter Passes

all frequency components

of the input signal witho-

ut any attenuation and

provides desired phase shift at different frequencies of the input signal.

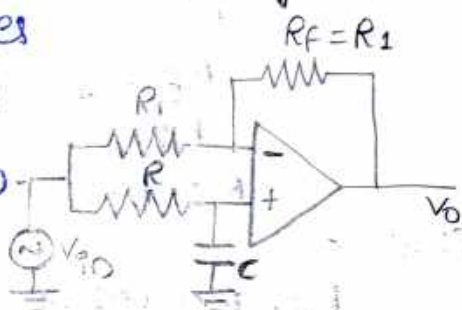
⇒ When signals are transmitted over transmission lines such as telephone wires they undergo change in phase. These phase changes can be compensated by All Pass Filter. Thus, All Pass Filter also called Delay equalizer (or) phase corrector.

$$V_o = -\frac{R_f}{R_i} V_i + V_+ \left(1 + \frac{R_f}{R_i} \right)$$

$$\text{Here } R_f = R_1, V_+ = \frac{V_i \times \frac{1}{SC}}{R + \frac{1}{SC}}$$

$$V_o = -\frac{R_f}{R_i} V_i + \frac{V_i \left(\frac{1}{SC} \right)}{\left(R + \frac{1}{SC} \right)} \left(1 + \frac{R_f}{R_i} \right)$$

$$= -V_i + 2V_i \left(\frac{1}{SCR + 1} \right)$$



put $S = j\omega$

$$V_o = V_i \left(\frac{2}{j\omega RC + 1} - 1 \right)$$

$$V_o = V_i \left(\frac{2 - j\omega RC - 1}{1 + j\omega RC} \right)$$

$$V_o = V_i \left(\frac{1 - j\omega RC}{1 + j\omega RC} \right)$$

$$\left| \frac{V_o}{V_i} \right| = \frac{\sqrt{1 + (\omega RC)^2}}{\sqrt{1 + (\omega RC)^2}}$$

$$\phi = 90^\circ$$

$$\left| \frac{V_o}{V_i} \right| = 1 \Rightarrow \phi = \tan^{-1} \left(\frac{\omega RC}{1} \right) - \tan^{-1} \left(\frac{\omega RC}{1} \right)$$

$$\phi = -2 \tan^{-1}(\omega RC)$$

The phase shift ϕ can be varied with frequency for a given resistor and capacitor and can be varied from 0 to -180° as they frequency is varied from 0 to ∞ .

$\Rightarrow$ The phase shift can be made positive by interchanging the R and C

Triangular wave generator:-

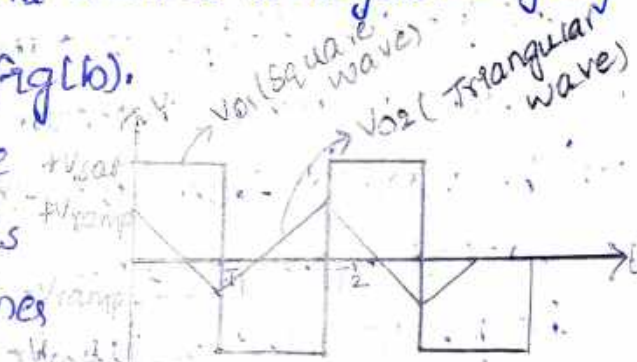


A triangular wave can be obtained by integrating the square wave. Here we are generating square wave form using comparator.

The circuit initially consists of comparator followed by an integrator. The output of comparator A_1 is a square wave of a amplitude $\pm V_{sat}$ & is applied to the inverting input terminal of the integrator A_2 producing Triangular wave.

This triangular wave is fed back as the input to comparator through voltage divider R_2, R_3 . Initially the output of comparator A_1 is $+V_{sat}$. The output of integrator A_2 will be a negative going Ramp as shown in fig(b).

Thus one end of the voltage divider R_2, R_3 is at a voltage $+V_{sat}$ & other at negative going ramp of A_2 .



At $t = t_1$ time, when the negative going ramp attains the value of $-V_{ramp}$, the effective voltage at point p becomes slightly less than zero volts. This switches the output of A_1 from positive saturation to negative saturation $-V_{sat}$. Similarly at $T = T_1$, the output of A_1 is from $-V_{sat}$ to $+V_{sat}$ & the output of A_2 is $-V_{ramp}$ to $+V_{ramp}$.

The amplitude of the triangular wave depends upon the R_C value of the integrator A_2 & the output voltage level of A_1 .

By writing the nodal equation at node p.

$$\frac{V_p - V_{o'}}{R_3} + \frac{V_p - V_o}{R_2} = 0$$

$$V_p \left(\frac{1}{R_3} + \frac{1}{R_2} \right) = \frac{V_{o'}}{R_3} + \frac{V_o}{R_2}$$

$$V_p \left(\frac{R_2 + R_3}{R_2 R_3} \right) = \frac{V_{o'}}{R_3} + \frac{V_o}{R_2}$$

$$V_{o'} = +V_{sat} \quad \& \quad V_o = -V_{ramp}$$

$$V_p \left(\frac{R_2 + R_3}{R_2 R_3} \right) = \frac{+V_{sat}}{R_3} + \frac{-V_{ramp}}{R_2}$$

$$V_p \left(\frac{R_2 + R_3}{R_2 R_3} \right) = \frac{V_{sat}}{R_3} - \frac{V_{ramp}}{R_2}$$

$$V_p = \frac{R_2}{R_2 + R_3} V_{sat} - \frac{R_3}{R_2 + R_3} V_{ramp}$$

$$\text{At } t = T_1, \quad V_p = 0$$

$$\frac{R_2}{R_2 + R_3} V_{sat} = \frac{R_3}{R_2 + R_3} V_{ramp}$$

$$V_{ramp} = \frac{R_2}{R_3} V_{sat}$$

Similarly

$$-V_{ramp} = -\frac{R_2}{R_3} V_{sat}$$

$$V_o = (+V_{ramp}) - (-V_{ramp})$$

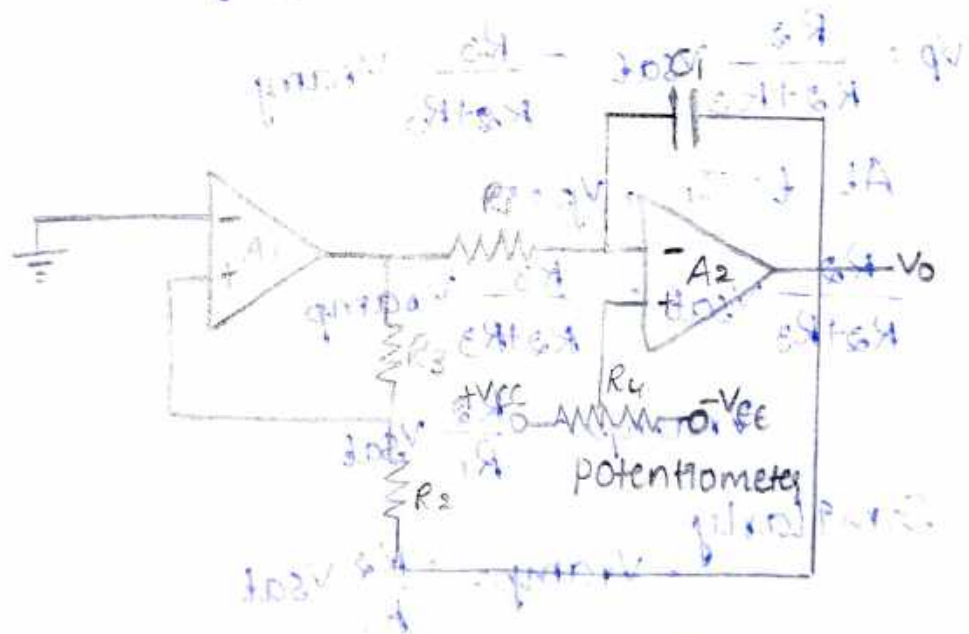
$$= \frac{R_2}{R_3} V_{sat} - \left(-\frac{R_2}{R_3} \right) V_{sat}$$

$$V_o = 2 \frac{R_2}{R_3} V_{sat}$$

Sawtooth Wave Generator

For triangular wave has equal rise and fall time ($t_r = t_f$) but sawtooth wave has unequal rise and fall time ($t_r \neq t_f$) i.e., it may rise positively many times faster than it falls negatively (or) vice versa ($t_r > t_f$) or ($t_r < t_f$).

The triangular wave generator can be converted to sawtooth wave generator by injecting a variable (potentiometer) by a DC voltage to the non-inverting terminal (+ve) of the integrator A_2 .



$t_r = t_f \Rightarrow$ Triangular wave



$\Rightarrow t_r > t_f$

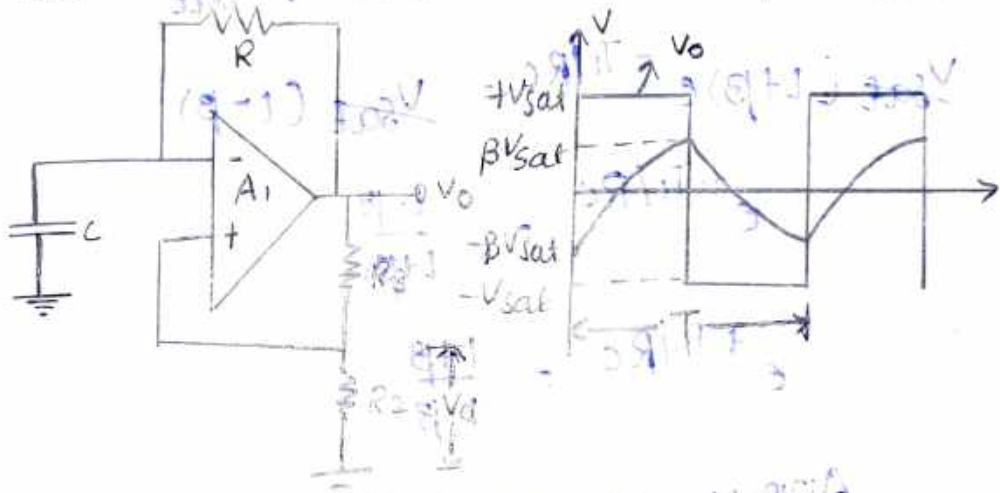


$\Rightarrow t_r < t_f$

* R_4 moves towards $-V_{ee}$ we get $t_r > t_f$.
 * R_4 resistor moves towards $+V_{cc}$ we get

$t_r < t_f$

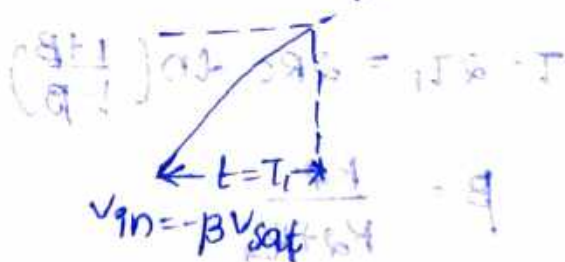
Square wave Generator (Astable Multivibrator) - Free running oscillator.



$$\beta = \frac{R_2}{R_2 + R_3}$$

$$V_c(t) = V_f + (V_{in} - V_f) e^{-t/RC}$$

$$V_c(T_1) = +\beta V_{sat} \quad V_f = V_{sat}$$



$$V_f = V_{sat}, \quad V_{in} = -\beta V_{sat}$$

$$V_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat}) e^{-t/RC}$$

$$= V_{sat} - V_{sat}(1 + \beta) e^{-t/RC}$$

$$\text{At } t = T_1, V_C(T_1) = \beta V_{\text{sat}}$$

$$V_C(T_1) = V_{\text{sat}} - V_{\text{sat}}(1+\beta)e^{-T_1/RC}$$

$$\beta V_{\text{sat}} = V_{\text{sat}} - V_{\text{sat}}(1+\beta)e^{-T_1/RC}$$

$$V_{\text{sat}}(1+\beta)e^{-T_1/RC} = V_{\text{sat}} - \beta V_{\text{sat}}$$

$$V_{\text{sat}}(1+\beta)e^{-T_1/RC} = V_{\text{sat}}(1-\beta)$$

$$e^{-T_1/RC} = \frac{1-\beta}{1+\beta}$$

$$e^{+T_1/RC} = \frac{1+\beta}{1-\beta}$$

Apply log on both sides

$$\frac{T_1}{RC} = \ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$T = T_1 + T_2 \quad (T_1 = T_2)$$

$$T = 2T_1 = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$\beta = \frac{R_2}{R_2 + R_3}$$

$$\text{If } R_2 = R_3$$

$$\beta = \frac{R_2}{2R_2}$$

$$\beta = 0.5$$

$$T = 2RC \ln \left(\frac{1+0.5}{1-0.5} \right)$$

$$= 2RC \ln \left(\frac{1.5}{0.5} \right)$$

$$T = 2RC \ln(3)$$

* It is a simple op-amp square wave generator (Astable multivibrator and free running oscillation).

* The principle of generation of square wave output: is to force an op-amp to operate in the saturation region. Then output voltage swings from $+V_{sat}$ to $-V_{sat}$ (or) $-V_{sat}$ to $+V_{sat}$ we get $V_o(p-p) = 2V_{sat}$.

* The reference voltage V_{ref} is βV_o and may take values as $+\beta V_{sat}$ or $-\beta V_{sat}$.

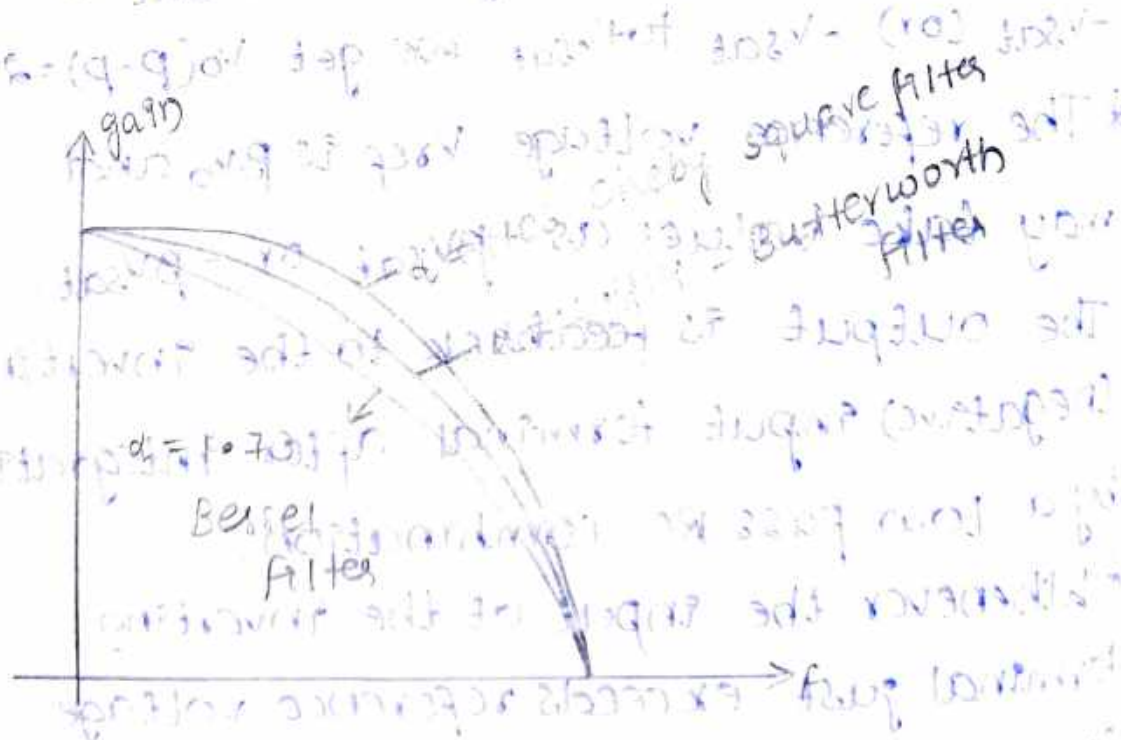
The output is feedback to the inverting (negative) input terminal after integrating by a low pass RC combination.

* Whenever the input at the inverting terminal just exceeds reference voltage ($V_{ref} = +\beta V_{sat}$) switching takes place resulting in a square wave output.

* If voltage across the inverting terminal just exceeds the BV_{sat} then we get $V_o = -V_{sat}$.

* If voltage across the non-inverting terminal exceeds the voltage across the inverting terminal (V_c) we get $V_o = +V_{sat}$. Like these the output may fluctuate from $+V_{sat}$ to $-V_{sat}$ and the voltage across the capacitor from $-V_{sat}$ to $+V_{sat}$.

Second Order Active Filter Response for different damping Coefficients (α)



IC 555 (Timer)

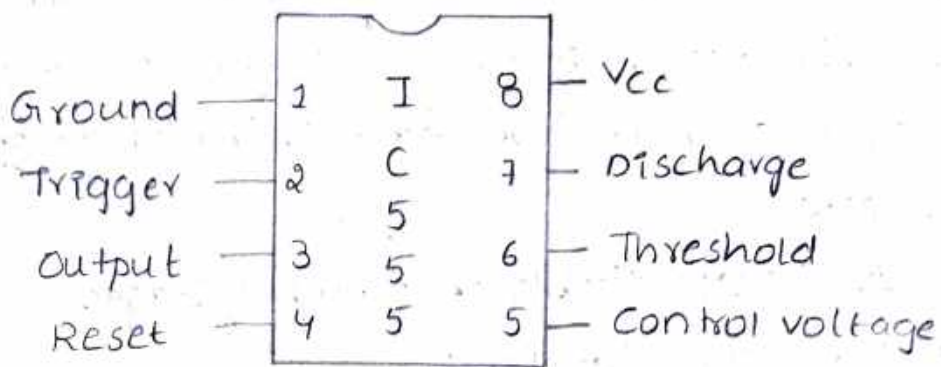
- * The 555 Timer is a highly stable device for generating accurate time delay or oscillations
- * Signetic corporation first introduced the device SEI NE 555 IC.
- * This IC is available in two packages.
 - 1) 8-pin circular package
 - 2) 8-pin DIP package & 14-pin DIP package.
- * The IC 556 Timer contains two 555 timers.
- * It's time delay ranging from μsec to hours and it can have maximum timing range of days.
- * The Supply voltage range is $+5\text{V}$ to $+18\text{V}$ and load current upto 200mA .
- * It is compatible with both TTL & CMOS logic circuits because of the wide range of supply voltage.

Features of 555 IC

Applications:-

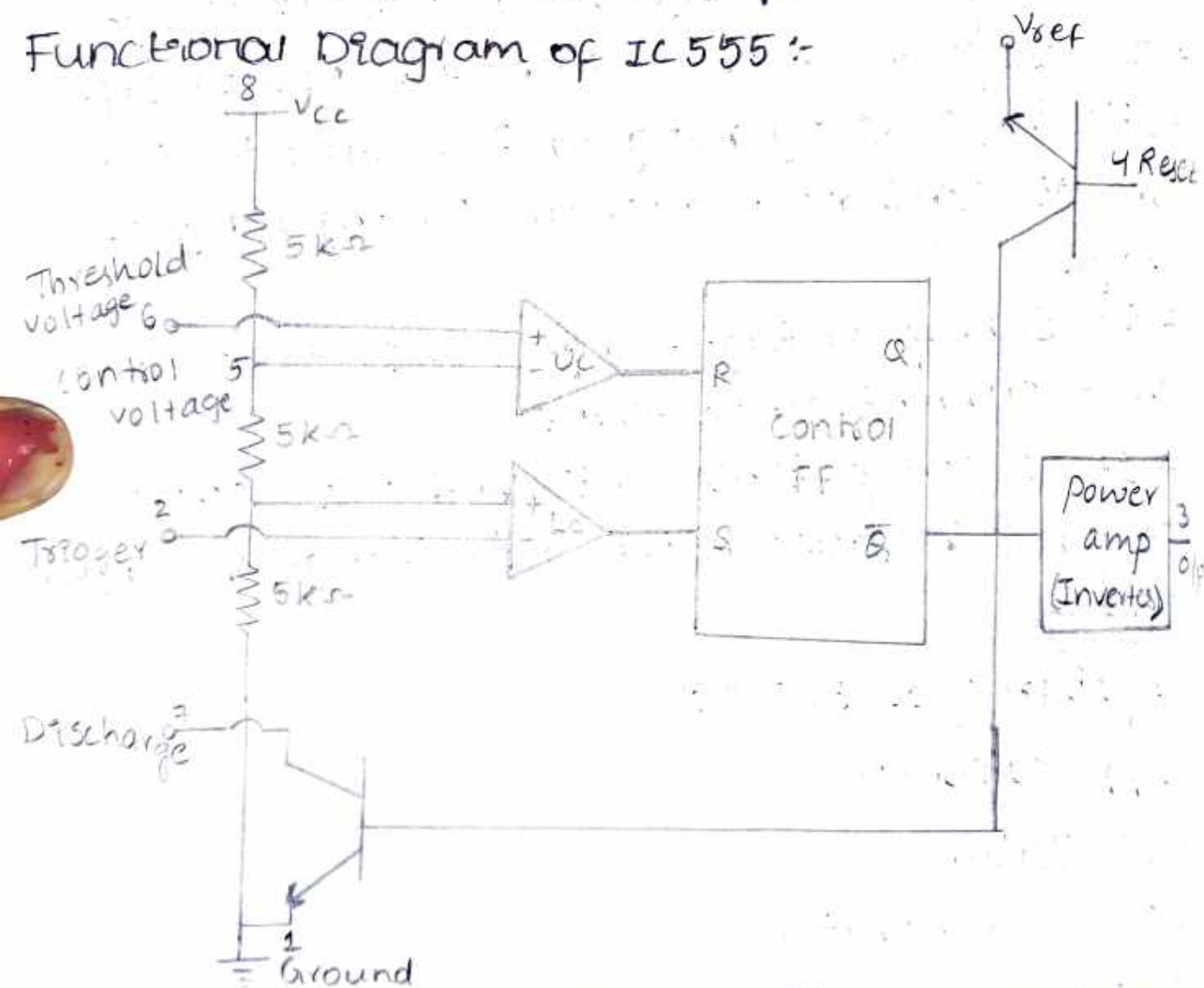
- 1) Oscillator
- 2) Pulse Generator
- 3) Square wave Generator (Astable Multivibrator)
- 4) Monostable Multivibrator (Monoshort Multi)
- 5) Ramp Generator
- 6) Burglar Alarm (In case of Navigation)
- 7) Traffic light control
- 8) Voltage Monitor, etc - - -

pin diagram of 555 IC :-

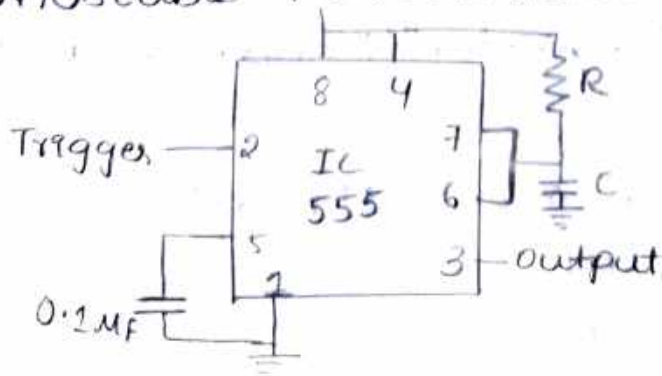


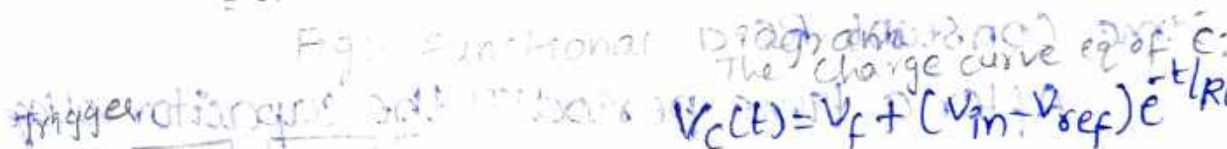
8-pin DIP Package IC 555

Functional Diagram of IC 555 :-



Monostable Multivibrator using IC 555





$$V_C(t) = V_{CC} + (0 - V_{CC})e^{-t/R_C}$$

$$V_c(t) = V_{CC}(1 - e^{-t/RC}) \quad \dots$$

$$\text{At } t = T \quad V_C(T) = \frac{2}{3} V_{CC}$$

$$2.11 - V_{RC} (1 - e^{-T/RC})$$

$$\frac{\partial V_{PC}}{\partial T} = \frac{V_{PC}}{T}$$

$$e^{i\pi/3} = \frac{1}{2} + i\frac{\sqrt{3}}{2}$$

$\tau_{RC} = \frac{1}{\omega_c} = \frac{1}{31.4}$

log on both sides

$$\Rightarrow T = R \ln 3$$

IT = IRRL

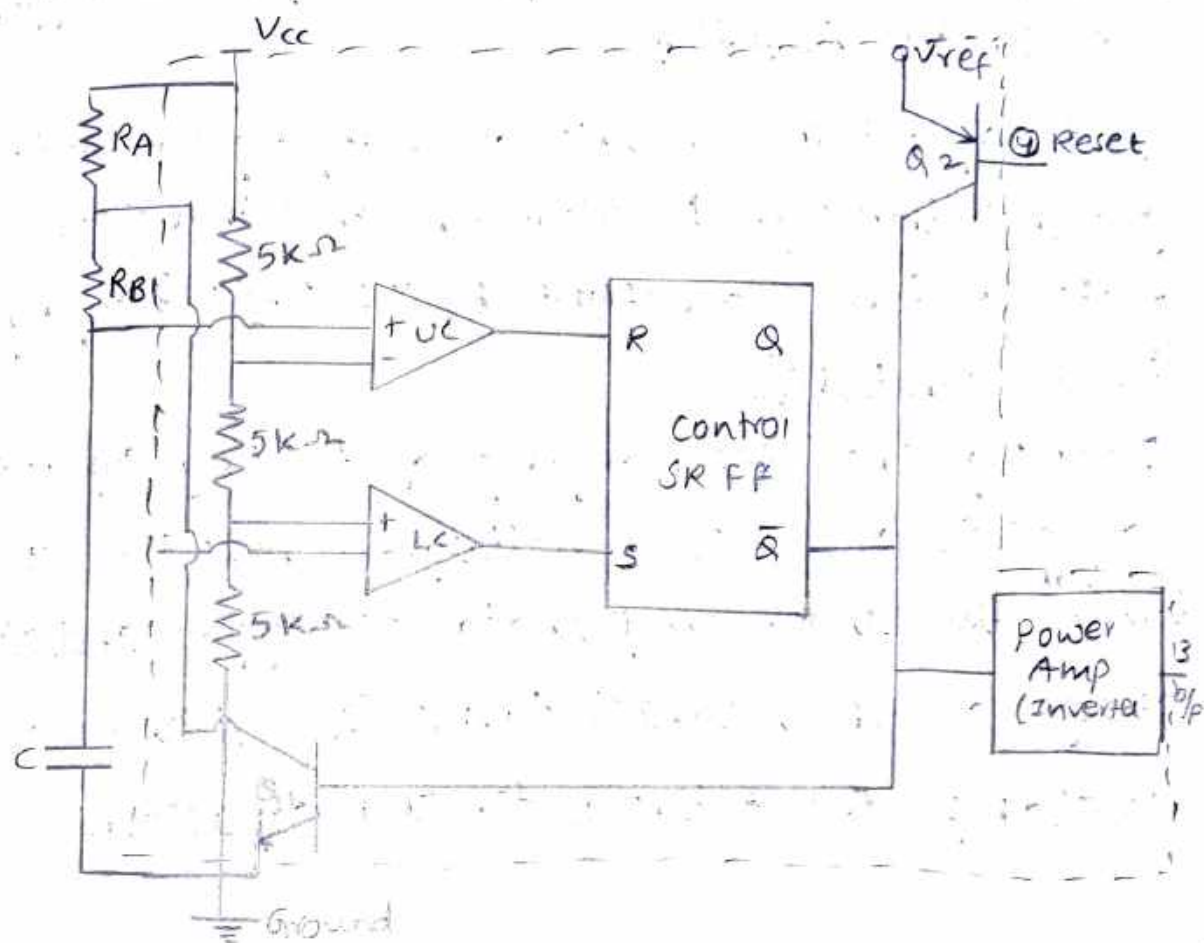
In the steady state flip flop holds the transistor Q_1 is in ON mode, thus clamping the external timing capacitor 'C' to ground. The output remains at ground potential.

As trigger passes through $\frac{V_{CC}}{3}$, ($V_+ < V_{CC}/3$) the lower comparator becomes set (1) so $S=1$ and $R=0$. The output of $\bar{Q}=0$. So output at pin 3 becomes high. This makes the transistor Q_1 off & the short circuit across the timing capacitor is released, now the capacitor is unclamped & voltage across it rises exponentially through resistor 'R' towards V_{CC} with a time constant RC .

After a time period 'T' the capacitor voltage is just greater than $2/3 V_{CC}$. The UC (generates) resets the flip flop i.e., $R=1$, $S=0$. This makes $\bar{Q}=1$ the transistor Q_1 goes on thereby discharging the capacitor 'C' rapidly to ground potential. The output returns to the standby state or ground potential.

By observing eqn) the timing interval 'T' is independent of supply voltage. It may be noted that once triggered the output remains in the high state until time 'T' completed which depends upon only the RC components. Any additional triggering pulse coming during this time will not change the old state.

Astable Multivibrator using IC 555:-



Functional diagram

Astable Multivibrator comparing with Mono-stable Multivibrator. Here the timing resistor is now split into two sections i.e., RA and RB. Pin 7 of discharging capacitor transistor Q1 is connected through the junction of RA & RB.

→ When the power supply V_{cc} is connected to the external timing capacitor C charges towards V_{cc} with a time constant $(RA + RB)C$.

→ During this time constant output at pin(3) is high = V_{cc} as Reset ($R=0$) and set ($S=1$), and this combination makes $\bar{Q}=0$, which has unclamped the timing Capacitor 'C'.

⇒ When the capacitor voltage equals or just greater than $\frac{2}{3}V_{CC}$. The upper comparator triggers the control flip flop

and capacitor C starts discharging towards a ground through Resistor R_B and transistor Q , with a time constant $R_B \times C$ [discharging time constant].

During the discharging of timing Capacitor C as it reaches a voltage across the capacitor less than $\frac{1}{3}V_{CC}$, the Lower comparator is triggered and at this stage $S=1, R=0$ which turns $\bar{Q}=0$. Now $\bar{Q}=0$ unclamps the external timing capacitor.

The capacitor thus periodically charged and discharged between $\frac{2}{3}V_{CC}$ and $\frac{1}{3}V_{CC}$ respectively.

$$V_C(t) = V_f + (V_{in} - V_f)e^{-t/RC}$$

$$V_C(t) = V_{CC}(1 - e^{-t/RC})$$

The time τ_1 taken by the circuit to charge from 0 to $\frac{2}{3}V_{CC}$

$$\text{at } t = \tau_1, V_C(t) = \frac{2}{3}V_{CC}$$

$$\frac{2}{3}V_{CC} = V_{CC}(1 - e^{-\tau_1/RC})$$

$$e^{-\tau_1/RC} = 1 - \frac{2}{3}$$

$$e^{-\tau_1/RC} = \frac{1}{3}$$

$$e^{+T_1/RC} = 3$$

Apply Natural log on both sides

$$\frac{T_1}{RC} = \ln 3$$

$$\boxed{T_1 = 1.1 RC}$$

⇒ Time taken by T_2 to charge from 0 to $1/3 V_{CC}$.

$$\text{at } t = T_2 \quad V_C(T_2) = 1/3 V_{CC}$$

$$1/3 V_{CC} = V_{CC} [1 - e^{-T_2/RC}]$$

$$e^{-T_2/RC} = 1 - \frac{1}{3}$$

$$= \frac{2}{3}$$

$$e^{T_2/RC} = 3/2$$

Apply N log on both sides

$$T_2/RC = \ln(3/2)$$

$$\boxed{T_2 = 0.405 RC}$$

Time to charge from $1/3 V_{CC}$ to $2/3 V_{CC}$.

$$t_{\text{high}} = T_1 - T_2$$

$$= 1.09 RC - 0.405 RC$$

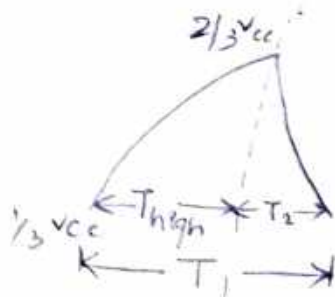
$$= 0.69 RC$$

$$t_{\text{high}} = 0.69 (R_A + R_B) C$$

$$t_{\text{low}} = 0.69 R_B C$$

$$T = t_{\text{high}} + t_{\text{low}}$$

$$\boxed{T = 0.69 (R_A + 2R_B) C}$$



$$f = \frac{1}{T}$$

$$= \frac{1}{0.69(R_A + 2R_B)C}$$

$$f = \frac{1.45}{(R_A + 2R_B)C}$$

∴ Duty cycle

$$\therefore D = \frac{t_{low}}{T}$$

$$= \frac{0.69R_B}{0.69(R_A + 2R_B)}$$

$$\therefore D = \frac{R_B}{(R_A + 2R_B)} \times 100$$

In a Monostable Multivibrator, $R = 100\text{ k}\Omega$, the time delay $T = 100\text{ ms}$. Calculate the value of the capacitor.

$$T = 1.09RC$$

$$\approx 1.1RC$$

$$R = 100\text{ k}\Omega$$

$$T = 100\text{ msec}$$

$$C = \frac{T}{1.1R}$$

$$= \frac{100 \times 10^{-3}}{1.1 \times 100 \times 10^3}$$

$$C = 0.9\text{ }\mu\text{F}$$

For $R_A = 6.8\text{ k}\Omega$, $R_B = 3.3\text{ k}\Omega$ and $C = 0.1\text{ }\mu\text{F}$, calculate T_{high} , T_{low} , free running frequency & Duty cycle

$$R_A = 6.8\text{ k}\Omega$$

$$R_B = 3.3k\Omega$$

$$C = 0.1\mu F$$

$$\begin{aligned} t_{high} &= 0.69(R_A + R_B)C \\ &= 0.69(6.8 + 3.3)10^3 \times 0.1 \times 10^{-6} \\ &= 0.69(10.1)10^{-3} \times 0.1 \\ &= 0.6969 \text{ msec} \end{aligned}$$

$$\begin{aligned} t_{low} &= 0.69 R_B C \\ &= 0.69(3.3 \times 10^3) \times 0.1 \times 10^{-6} \\ &= 0.69(3.3 \times 0.1) \times 10^{-3} \\ &= 0.2277 \text{ msec} \end{aligned}$$

$$\begin{aligned} f &= \frac{1}{T} = \frac{1}{0.6969(6.8 + 2(3.3))10^3 \times 0.1 \times 10^{-6}} \\ &= \frac{1}{0.69(6.8 + 6.6) \times 0.1 \times 10^{-3}} \\ &= \frac{1}{0.9246 \times 10^{-3}} \\ &= \frac{1}{0.9246 \text{ msec}} \end{aligned}$$

$$\boxed{f = 1.08 \text{ kHz}}$$

$$\begin{aligned} \text{Duty cycle} &= \frac{3.3k}{(6.8k + 6.6k)} \\ &= 0.25 \end{aligned}$$

$$\boxed{\%D = 25\%}$$

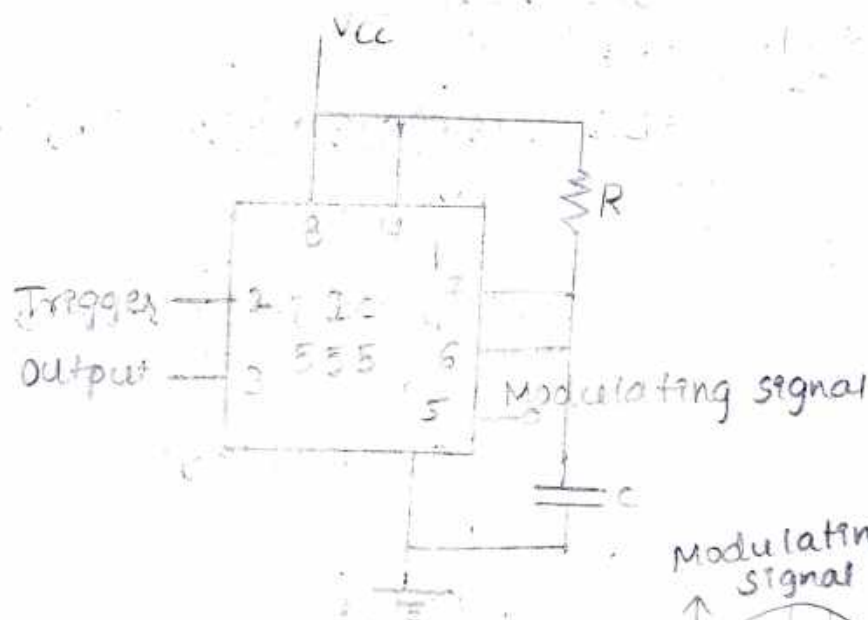
Applications of Monostable Multivibrator

1. Pulse width Modulation
2. Missing pulse detector
3. Linear Ramp Generator
4. Frequency divider

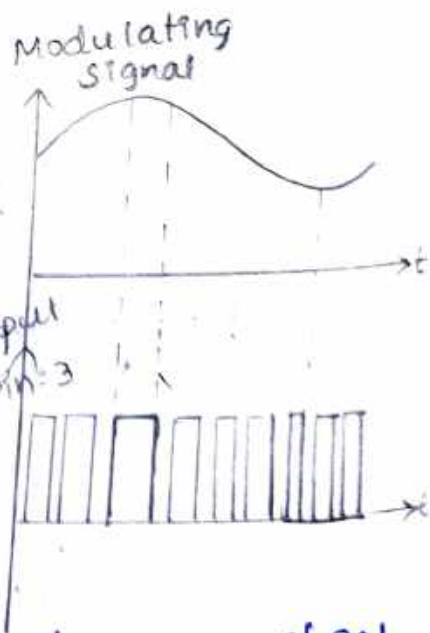
Applications of Astable Multivibrator

1. Frequency Shift Keying (FSK) generator
2. Pulse Position Modulation (PPM)

Pulse Width Modulator

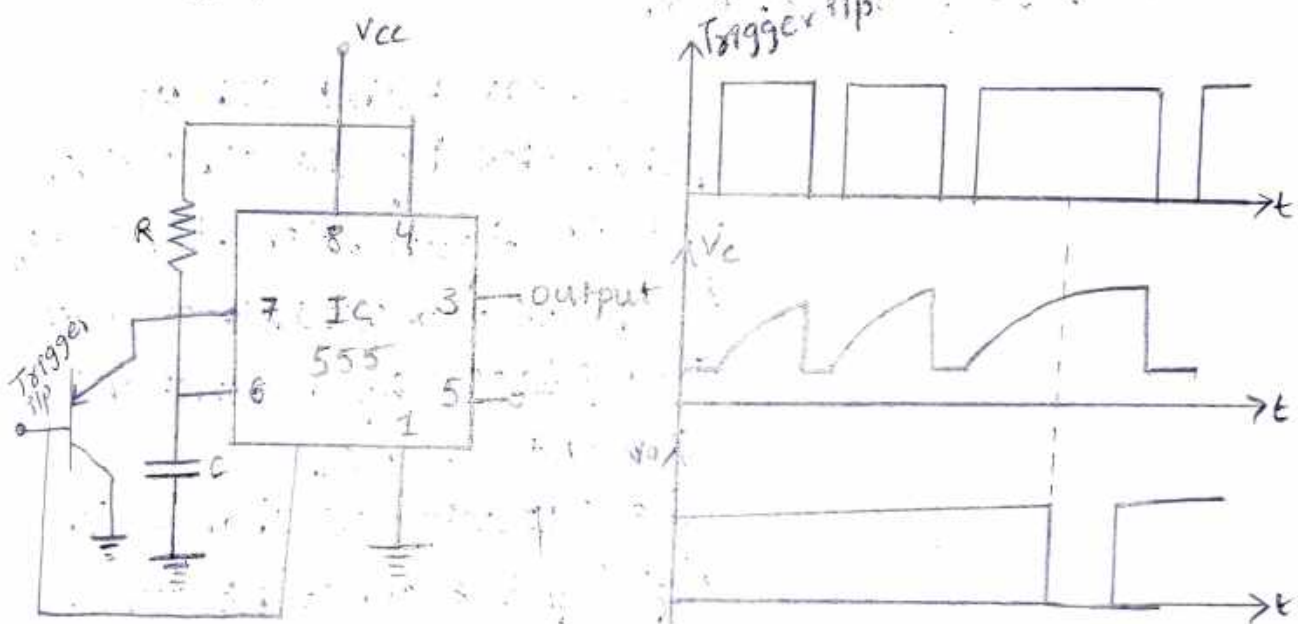


This is basically a monostable multivibrator with a modulating input signal applied at Pin-5. By the application of continuous trigger at pin-2. A series of pulses are obtained, the duration of which depends on the modulating input at pin-5.



The Modulating signal applied at pin-5 gets superimposed on the already existing voltage $\frac{2}{3}V_{CC}$ at the inverting input terminal of the upper comparator. This in turn changes the threshold level of the upper comparator and output PWM at pin-3.

Missing pulse Detector



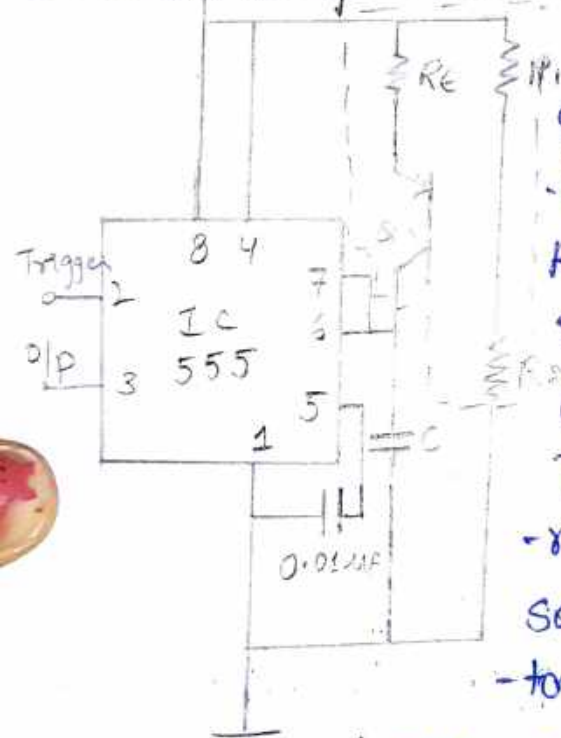
In this circuit input trigger is low, the emitter diode of Transistor A is forward bias. The Capacitor C gets clamped to cut-in voltage of the transistor ($V_{in} = 0.7$ for silicon) the output of the timer goes high ($LC = Set (S) = 1, S = 1, Q = 1, \bar{Q} = 0$). The circuit is designed so that the time period of monostable circuit is slightly greater than the trigger pulse. So long the trigger pulse train keeps coming at pin-2. The output remains high. However if a pulse misses, the trigger input is high, the transistor A is cut-off. Now the

timer enters into a normal state of monostable operation. The output goes low after a time T of the monoshot.

Applications :-

- 1, To detect the missing heartbeat in medical environment
- 2, To control speed of rotating wheel.

Linear Ramp Generator



Linear ramp can be generated by the circuit shown in figure. Here, the resistor R of the monostable circuit is replaced by a constant current source.

The capacitor is charged linearly by the constant current source formed by the transistor Q_2 . The capacitor voltage

V_C can be written as $V_C = \frac{1}{C} \int_0^t i \, dt \quad (1)$

where, i is the current supplied by the constant current source.

$$-V_{BE} + \frac{R_1}{R_1 + R_2} V_{CC} = I_E R_E$$

$$\frac{R_1 V_{CC} - V_{BE} (R_1 + R_2)}{R_1 + R_2} = [I_B + I_C] R_E$$

$$= [I_B + \beta I_B] R_E$$

$$= [I_B (1 + \beta)] R_E \quad \beta \gg 1$$

$$= (\beta I_B) R_E$$

$$= I_C R_E$$

$$\frac{R_1 V_{CC} - V_{BE} (R_1 + R_2)}{(R_1 + R_2) R_E} = I$$

Now substitute I in eq(1)

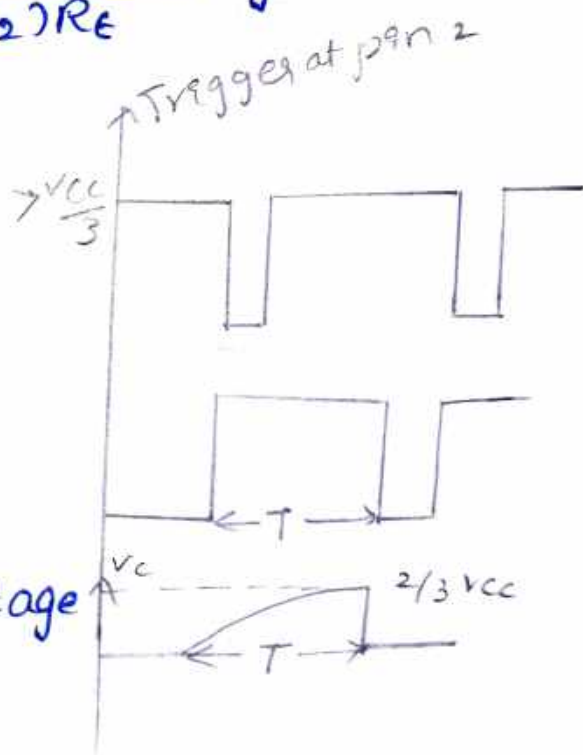
$$V_C = \frac{1}{C} \int_0^t \left[\frac{R_1 V_{CC} - V_{BE} (R_1 + R_2)}{(R_1 + R_2) R_E} \right] dt$$

$$= \frac{1}{C} \left[\frac{R_1 V_{CC} - V_{BE} (R_1 + R_2)}{(R_1 + R_2) R_E} \right] t$$

$$\text{At } t = T \quad V_C(t) = \frac{2}{3} V_{CC}$$

$$\frac{2}{3} V_{CC} = \frac{1}{C} \left[\frac{R_1 V_{CC} - V_{BE} (R_1 + R_2)}{(R_1 + R_2) R_E} \right] T$$

The capacitor discharges as soon as the voltage reaches $\frac{2}{3} V_{CC}$ which is threshold voltage of the upper comparator in the monostable circuit of the functional diagram. The capacitor voltage is zero till another trigger is applied.

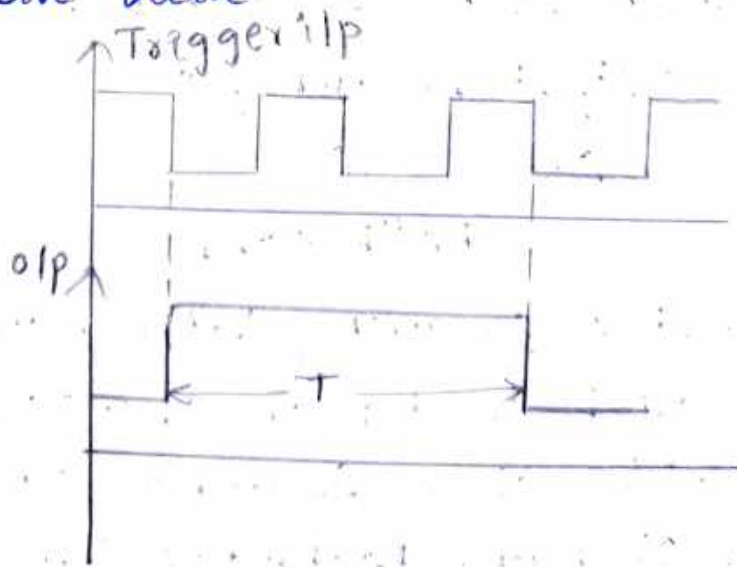


Frequency Divider :-

A continuously triggered monostable circuit is trigger by square wave generator can be used as frequency divider. If the timing interval is adjusted to longer than the period of triggering square wave input signal.

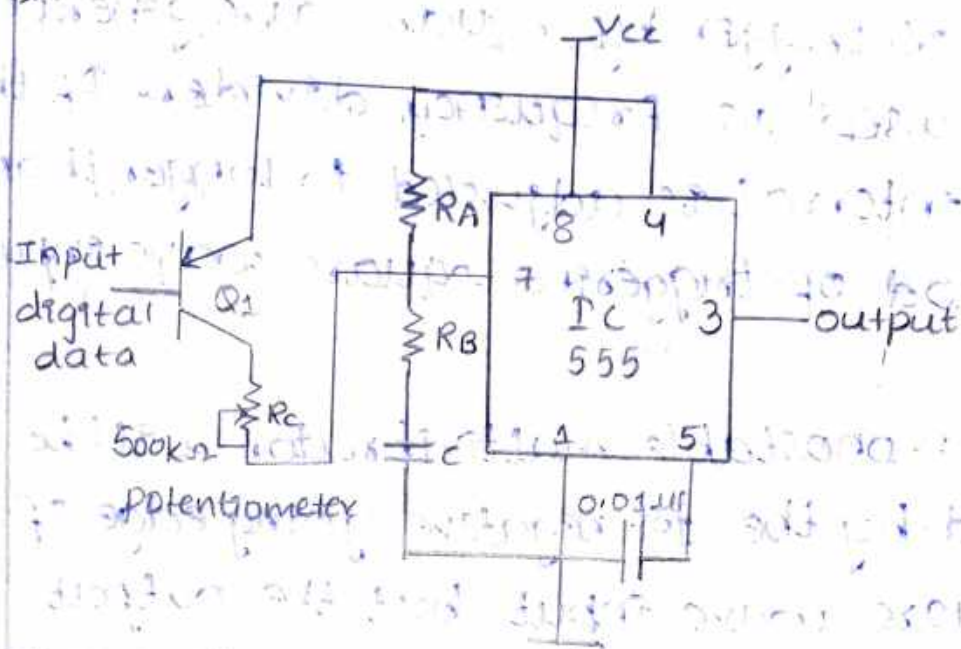
The monostable multivibrator will be triggered by the 1st negative going edge of the square wave input but the output will remain high for next negative going edge of the input square wave as shown in figure.

The monoshot will however be triggered on 3rd negative going input depending on the choice of time delay. In this way the output will be made integral fraction of the frequency of the input triggering square wave.



Applications of Astable Multivibrator

1) FSK Generator:-



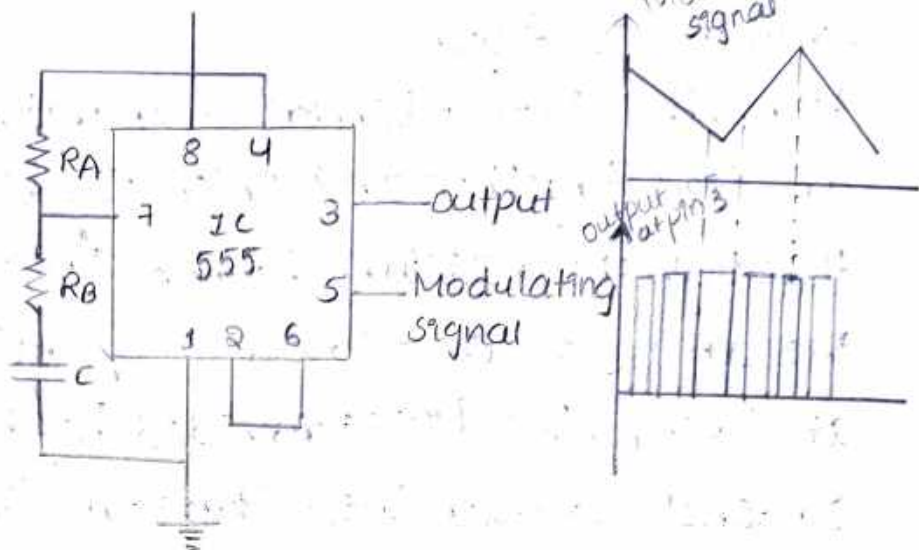
→ When the input digital data is high the transistor Q_1 becomes OFF in this condition. The IC 555 works in normal astable multivibrator mode of operation. So, the frequency of output waveform is $f = \frac{1.45}{\left(\frac{R_A}{R_B} + 2R_B\right)C}$. When

the input data is low the transistor Q_1 becomes ON & it acts like a short circuit. In this condition, the resistance R_C is in parallel with R_A . So, the output frequency is

$$f = \frac{1.45}{(R_A || R_C + 2R_B)C}$$

In MODEM, the frequency between 1070 Hz to 1270 Hz can be used as one of the standard FSK signals. The above frequencies can be selected by changing R_A , R_B , R_C & C .

2) Pulse Position Modulator:-

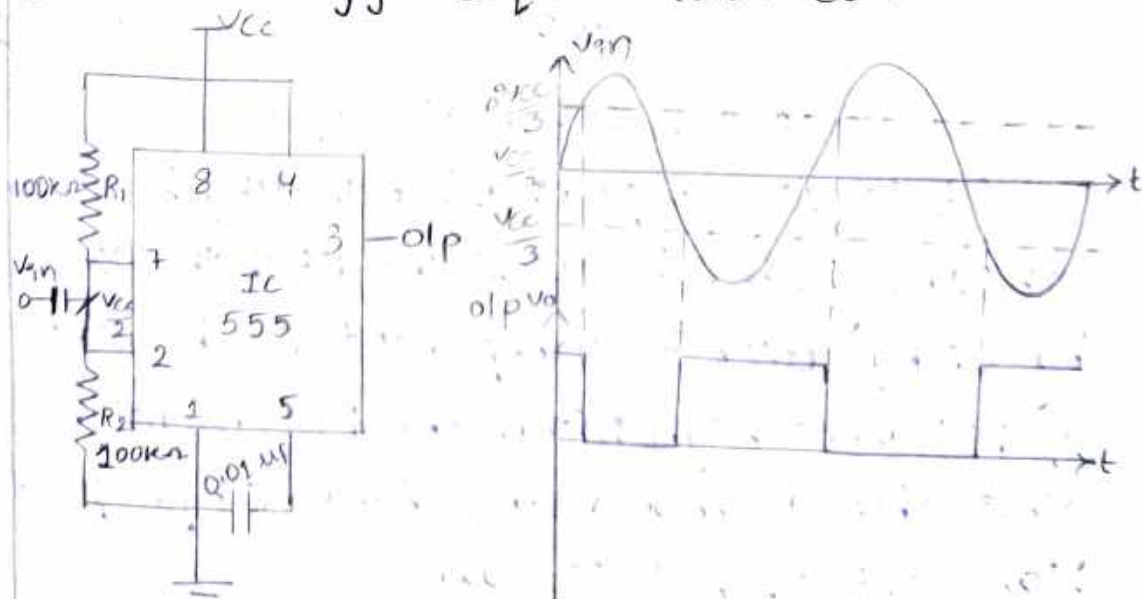


This can be constructed by applying a modulating signal to pin-5 of the 555 timer connected in astable mode.

The output pulse position varies with modulating signal since the threshold voltage & hence the time delay is varied.

It may be noted from the output waveform that the frequency is varying that we are observed in the PPM signal.

Schmitt Trigger (square wave converter):-



The use of 555 timer as a schmitt trigger shown in figure.

Here, the two internal comparators (U_C & L_C) are tied together and externally biased at $\frac{V_{CC}}{2}$ through the resistors R_1 & R_2 . Since, the U_C will trip at $\frac{2}{3}V_{CC}$ and lower comparator will trip at $\frac{1}{3}V_{CC}$, the bias provided by R_1 & R_2 are centered with in these three two threshold voltages. Thus, sine wave of sufficient amplitude $\left[\left(> \frac{V_{CC}}{6} \right) \Rightarrow \frac{2}{3}V_{CC} - \frac{V_{CC}}{2} \right]$ to exceed the reference levels causes the internal FF to alternately set and Reset, providing a square wave as a output.

Phase Locked Loop [PLL]:-

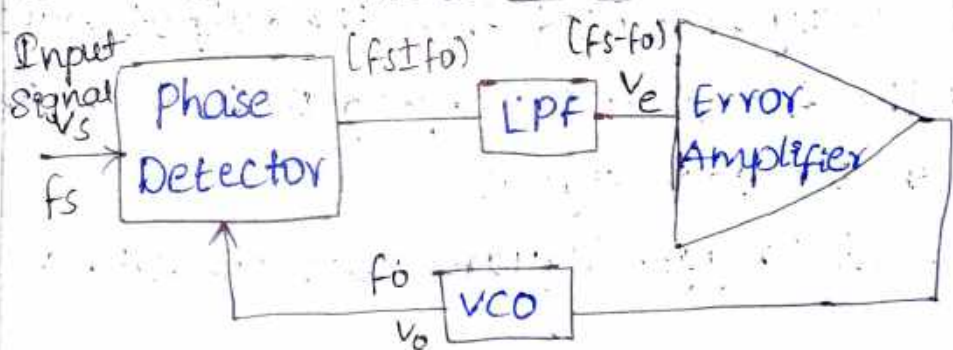


Fig:- Block Schematic of PLL

It is an important building block or linear system. This was invented in 1930's by using discrete components so the cost of PLL was high. Now, the PLL must be available in monolithic form (single piece). Now cost of PLL is low.

Applications of PLL;

1. RADAR synchronization & communication application.

2. Satellite Communication

3. Airborne navigation system.

4. FM communication system.

5. It is also used in computers etc.

The block diagram of PLL consists of phase detector/comparator/multiplier, LPF, error amplifier, voltage controlled oscillator [VCO].

The VCO is a free running multivibrator and operates at a set of frequencies f_0 called free running frequency. This frequency is determined by external timing resistors & capacitor. It can be shifted either side by applying a DC controlled voltage V_c to an appropriate terminals of IC.

The frequency deviation is directly proportional to the DC controlled voltage & hence it is called a voltage controlled oscillator [VCO].

If an input signal of amplitude V_s frequency f_s is applied to the PLL, the phase detector compares the phase & frequency of the incoming signal to that of the output voltage V_o of the VCO. If the two signals differ in frequency & phase an error voltage

' V_e ' is generated. The phase detector is basically a multiplier & produces the sum ($f_s + f_o$) & difference ($f_s - f_o$) components at its output. The high frequency component $f_s + f_o$ is removed by LPF & difference frequency $f_s - f_o$ (low freq) is amplified & then applied as controlled voltage V_c to VCO.

The signal V_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s & f_o . Once this action starts we say that the signal is in the capture range. The VCO continues to change in frequency till its output frequency is exactly same as the input frequency ($f_o = f_s$). The circuit is then said to be locked. Once locked the output frequency f_o of VCO is identical to f_s except for a finite phase difference. The phase difference (ϕ) generates a corrective controlled voltage to shift the VCO frequency from f_o to f_s & they may maintain the 'lock range'.

The range of frequency over which the PLL can maintain lock with the incoming signal is called Lock in Range or track in range.

The range of frequency over which the PLL can acquire lock with the input,

signal is called 'capture range'.

The total time taken by PLL to establish lock is called Pull-in time. This depends on the initial phase & frequency difference between the signals (f_s, f_o) as well as on the overall loop gain & LPF characteristics.

Types of Phase Detector:-

There are 2 types of phase detectors

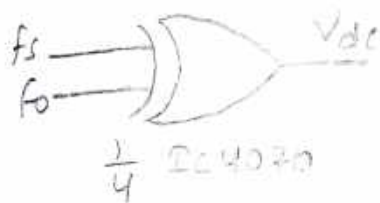
1. Analog phase detector

2. Digital phase detector

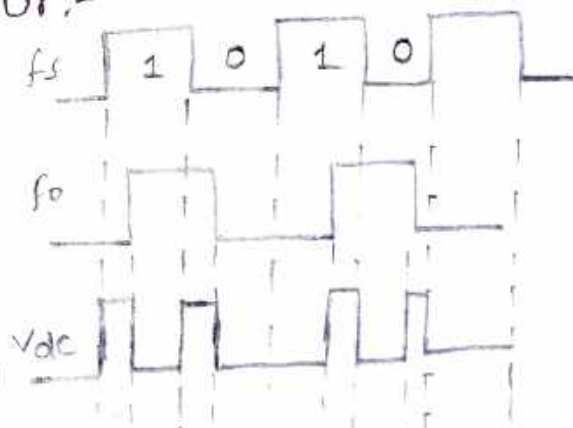
Electronic switch type PD
Balanced modulator type PD

EX-OR gate phase detector
Edge triggered type PD.

EX-OR phase Detector:-



Fig(a) EX-OR PD



Fig(a) shows digital type EX-OR phase detector. It uses CMOS two input EX-OR gate. The output of the EX-OR gate is high when only one of the input signal f_s or f_o is high. This type of detector is used when both the input signals are square waves. The input and output waveforms are shown in fig(b). In this fig(b) f_s is leading f_o by π phase difference.

The variations of a DC output voltage with phase difference is shown in fig(c). It can be seen that the max DC output voltage occurs when the phase difference is π . Because the output of the gate remains high.



use the output of the gate remains high.

→ The slope of the curve is k_{π} .

Voltage Controlled Oscillator - VCO → (Nelson)

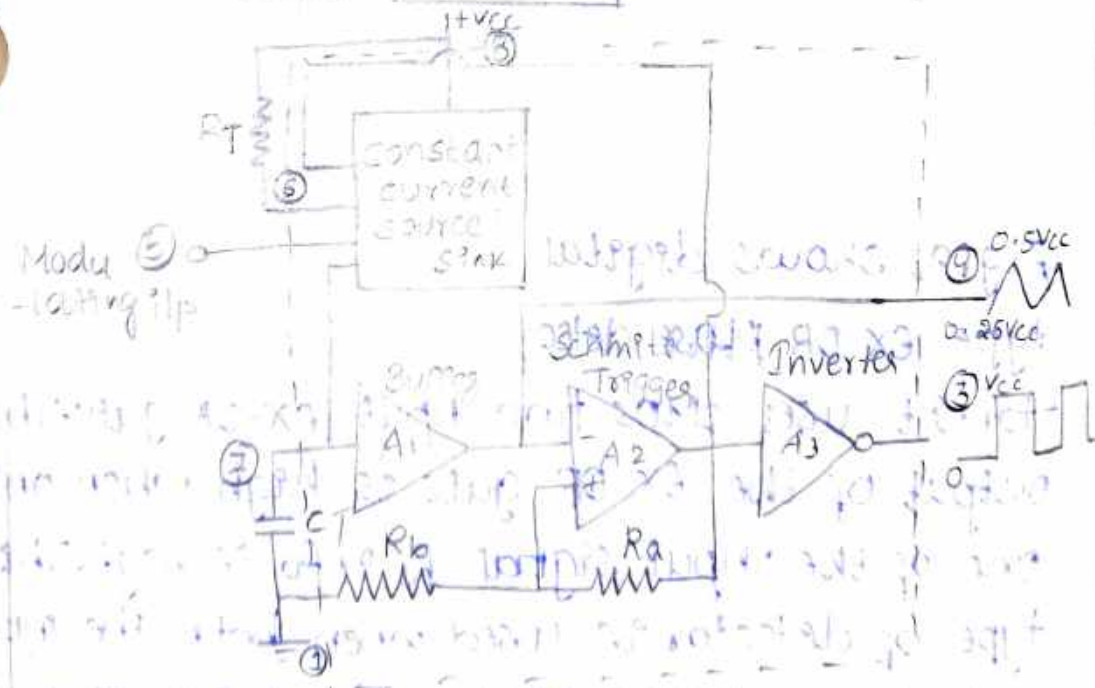
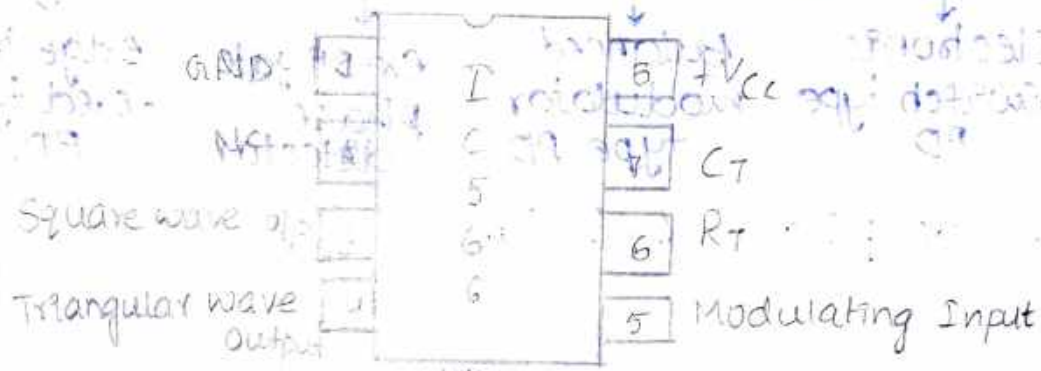


Fig. Functional Diagram of VCO

Voltage Controlled Oscillator is available in IC form as $\mu\text{C}101$ or $\mu\text{C}105$.

The timing capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage V_C applied at the modulating input (pin-5) or by changing the timing resistor R_T external to the IC. The voltage at pin-6 is held at the same voltage as pin-5. Thus, if the modulating voltage at pin-5 increases then the voltage at pin-6 also increases resulting in less voltage

A small capacitor of $0.001 \mu\text{F}$ should be connected between pin-5 & pin-6 to eliminate possible oscillations.

The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt Trigger A_2 via Buffer amplifier A_1 .

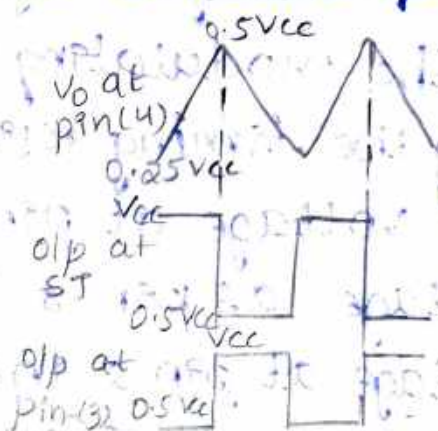
The output voltage of Schmitt trigger is designed to $0.5V_{CC}$ to V_{CC} .

If $R_A = R_B$ in the positive feedback loop, the voltage at the non-inverting terminal of A_2 swings from $0.25V_{CC}$ to $0.5V_{CC}$.

→ When the voltage across the capacitor $V_{C_T} > 0.5V_{CC}$ during charging the output of the Schmitt Trigger goes low [$0.5V_{CC}$].

→ The capacitor now discharges when it is at $0.25V_{CC}$. The output of Schmitt Trigger goes high $[V_{CC}]$.

→ Since the source and sink currents are equal the capacitor C_T charges and discharges for the same amount of time.



The output frequency of VCO:-

The control voltage [voltage across capacitor / Modulating input] changes from $0.25V_{CC}$ to $0.5V_{CC}$.

$$\Delta V = 0.25V_{CC}$$

The capacitor charges with a constant current source (sink).

$$Q = CV, Q = it$$

$$CV = it$$

$$C \Delta V = i \Delta t$$

$$\boxed{\frac{\Delta V}{\Delta t} = \frac{i}{C_T}}$$

Substitute $\Delta V = 0.25V_{CC}$ in above

$$\frac{0.25V_{CC}}{\Delta t} = \frac{i}{C_T} \Rightarrow \boxed{\Delta t = \frac{0.25V_{CC} C_T}{i}}$$

The time period of triangular waveform equal to $2\Delta t$.

The frequency of oscillator, $f_0 = \frac{1}{T}$

$$= \frac{1}{2\Delta t} = \frac{1}{2 \times 0.25 V_{CC} C_T} \Rightarrow \frac{1}{0.5 V_{CC} C_T}$$

But $q = \frac{V_{CC} - V_C}{R_T}$

$$f_0 = \frac{\left(\frac{V_{CC} - V_C}{R_T} \right)}{0.5 V_{CC} C_T}$$

$$f_0 = \frac{2(V_{CC} - V_C)}{V_{CC} R_T C_T}$$

The output frequency of VCO can be changed by changing the R_T , C_T and V_C .

The voltage at pin-5, $V_C = V_{pin5} = \frac{7}{8} V_{CC}$

$$f_0 = \frac{2(V_{CC} - \frac{7}{8} V_{CC})}{V_{CC} R_T C_T}$$

$$= \frac{2 \times \frac{V_{CC}}{8}}{V_{CC} R_T C_T} = \frac{0.25}{R_T C_T}$$

$$f_0 = \frac{0.25}{R_T C_T}$$

Voltage to Frequency Conversion factor:-

[kV]:-

$$k_V = \frac{\Delta f_0}{\Delta V_C} \quad (1)$$

$$\Delta f_0 = f_1 - f_0$$

$$= \frac{2(V_{CC} - V_C + \Delta V_C)}{V_{CC} R_T C_T} - \frac{2(V_{CC} - V_C)}{V_{CC} R_T C_T}$$

$$\Delta f_o = \frac{2\Delta V_c}{V_{CC} R_T C_T}$$

Substitute Δf_o in eqn)

$$K_V = \frac{\frac{2\Delta V_c}{V_{CC} R_T C_T}}{\Delta V_c}$$

$$= \frac{2}{V_{CC} R_T C_T}$$

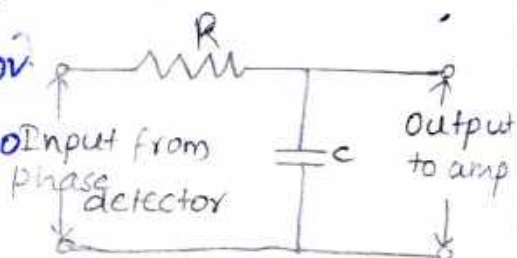
Substitute $R_T C_T = \frac{0.25}{f_o}$

$$K_V = \frac{2}{V_{CC} \times \frac{0.25}{f_o}}$$

$$K_V = \frac{8f_o}{V_{CC}}$$

LPF (LOW Pass Filter) :-

→ The LPF not only removes high frequency components and noise but



also controls the dynamic characteristics of PLL.

→ These characteristics include capture, lock range, Bandwidth, Transient response

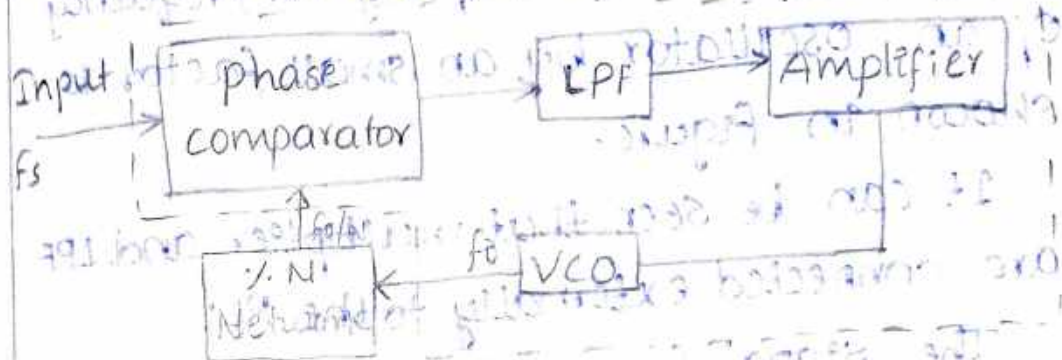
→ If filter Bandwidth is reduced then the response time increases. However reducing the Bandwidth of the filter also reduces the lock & capture range of PLL.

→ The charge on the filter capacitor gives short time memory for the PLL.

PLL Applications:

- 1) Frequency Multiplier / Divides
- 2) Frequency translation
- 3) AM detection
- 4) FM demodulation
- 5) FSK demodulator

Frequency Multiplication / Division:



In this block diagram, a divider by N network is inserted between the VCO output and phase comparator input.

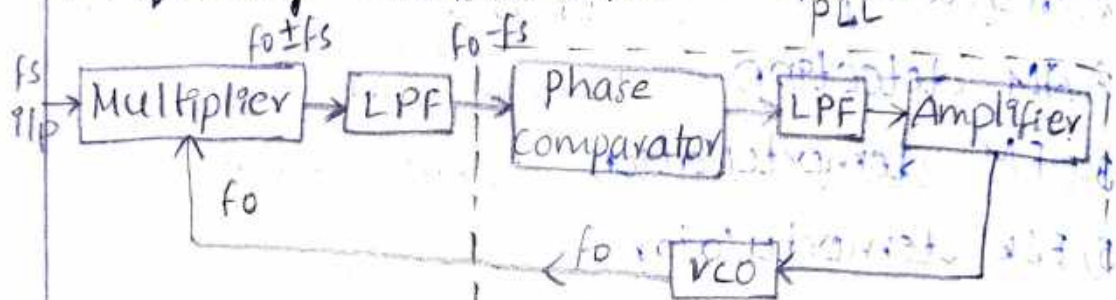
In the locked state the VCO output frequency f_o is given by $f_o = N f_s$.

This Multiplication can be obtained by selecting a proper scaling factor N of the counter.

The circuit can also be used for frequency division. Since, the VCO output is rich harmonics. It is possible to lock the m th harmonic of the VCO output with the input signal f_s . The output f_o of VCO is $f_o = \frac{f_s}{M}$.

$$f_o = \frac{f_s}{m}$$

Frequency Translation



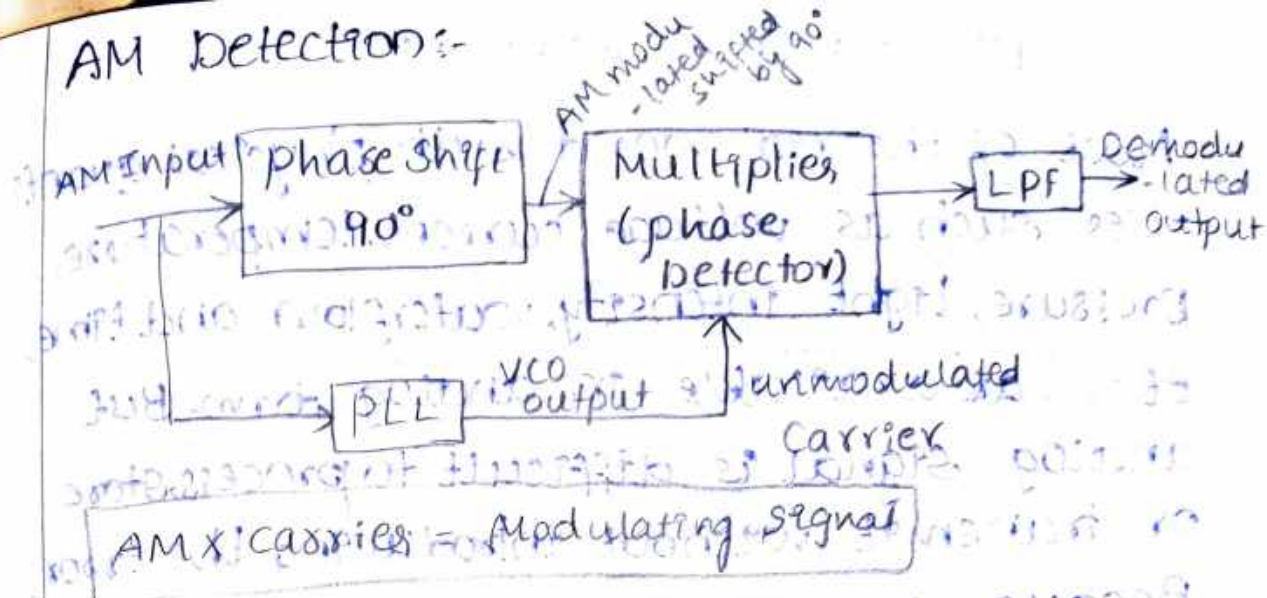
A Schematic for shifting the frequency of an oscillator by an small factor is shown in figure.

It can be seen that multiplier and LPF are connected externally to the PLL.

The signal f_s which has to be shifted and the output frequency of vco are applied as inputs to the multiplier. The output of the multiplier contains sum and difference of f_s & f_o . However the output of LPF contains only the difference signal $f_s - f_o$.

The translation/offset frequency f_1 is applied to the phase comparator. When PLL is in locked state $f_o - f_s = f_1$ (or) $f_o = f_s + f_1$. Thus, it is possible to shift the incoming frequency f_s by f_1 .

AM Detection:-



A PLL may be used to demodulate AM signals as shown in figure. The PLL is locked to the carrier frequency of the incoming AM signal. The output of VCO which has the same frequency as the carrier but this is unmodulated carrier is fed to the multiplier. Since, VCO output is always 90° phase with the incoming AM signal under the locked condition. The AM input signal is also shifted in phase by 90° before being fed to the multiplier.

This makes the both signals applied to the multiplier are in same phase. The output of the multiplier contains sum & difference signal. These signals we are applied to the LPF it allows only the low frequency signal that is nothing but demodulated output as a message signal.

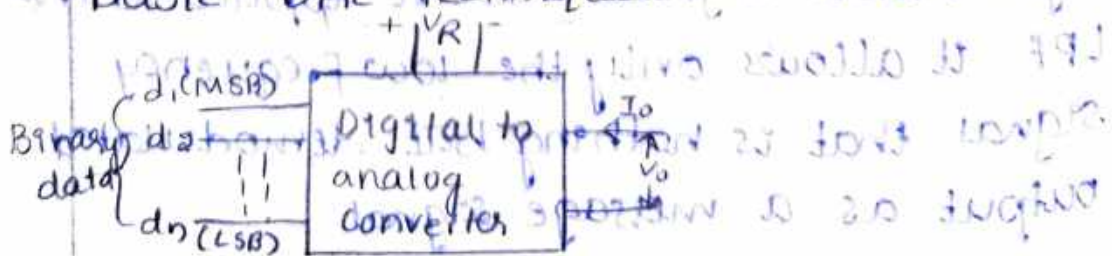
III - DATA CONVERTERS

Most of the real world with physical quantities such as voltage, current, temperature, pressure, light intensity, waterflow and time, etc. are available in analog form. But analog signal is difficult to process, store or transmit without introducing the error. Because of superimposition of noise, in case of amplitude modulation. So, for processing, transmission and for storage purpose it is convenient to use digital signals. It gives better accuracy and reduces the noise.

Applications:-

- 1) Digital Audio recording & playback
- 2) In computer systems.
- 3) Music & video Syntheses.
- 4) Digital Multimeters
- 5) Digital signal processing
- 6) Pulse Code Modulation transmission
- 7) Microprocess based instrumentation.

Basic DAC techniques



Schematic of DAC

$$V_o = K V_{FS} (d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \dots - d_n 2^{-n})$$

→ The input is n -bit binary word (data) is combined with reference voltage V_R to give an analog output signal.

→ The output of DAC can be either voltage or current for voltage output DAC the DAC converter is mathematically described as

$$V_o = k V_{FS} [d_1 2^{-1} + d_2 2^{-2} + \dots - d_n 2^{-n}]$$

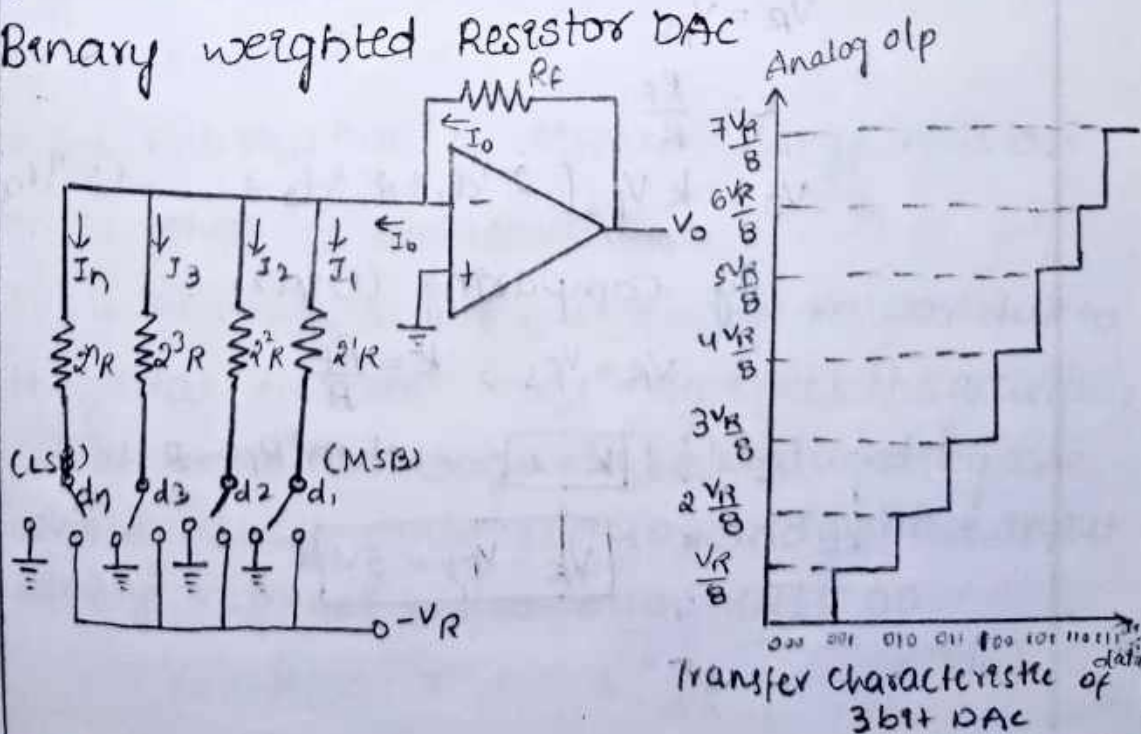
where V_o is a output voltage, V_F is Full scale output voltage $[5V]$, k is a scaling factor usually adjusted to unity $d_1 - d_n$.

d_1 is the [MSB] with a weight of $\frac{V_{FS}}{2}$
 d_n is the [LSB] with a weight of $\frac{V_{FS}}{2^n}$

Types of DAC:-

- 1) Binary weighted Resistor DAC
- 2) R-2R ladder DAC
- 3) Inverted R-2R ladder DAC.

Binary weighted Resistor DAC



The circuit uses inverting summing amplifier with a binary weighted resistor network. It has a n-electronic switches $d_1, d_2, \dots, d_n$ controlled by binary input word or data. These switches are SPDT (Single Pole Double Throw).

- If the binary input to particular switch is '1' it connects the resistor to the reference voltage V_R .
- If the input bits are zero the switch connects resistor to ground.
- If the output current (I_O) for an ideal op-amp can be written as

$$I_O = I_1 + I_2 + I_3 + \dots + I_n$$

$$= \left[\frac{-V_R}{2^1 R} \right] d_1 + \left[\frac{-V_R}{2^2 R} \right] d_2 + \left[\frac{-V_R}{2^3 R} \right] d_3 + \dots + \left[\frac{-V_R}{2^n R} \right] d_n$$

$$= \frac{-V_R}{R} \left[2^{-1} d_1 + 2^{-2} d_2 + 2^{-3} d_3 + \dots + 2^{-n} d_n \right]$$

$$V_O = -I_O R_f$$

$$V_O = + V_R \frac{R_f}{R} \left[2^{-1} d_1 + 2^{-2} d_2 + \dots + 2^{-n} d_n \right] \quad (1)$$

$$V_R = V_{FS}$$

$$k = \frac{R_f}{R}$$

$$V_O = k V_{FS} \left[2^{-1} d_1 + 2^{-2} d_2 + \dots + 2^{-n} d_n \right] \quad (2)$$

By comparing (1) & (2)

$$V_R = V_{FS}, \quad k = \frac{R_f}{R}$$

$$\boxed{k = 1}, \text{ when } R_f = R$$

$$\boxed{V_R = V_{FS} = 5V}$$

If reference voltage is negative we get analog output voltage is positive staircase & vice versa.

This circuit we can connect in non-inverting mode also.

This circuit acts as a current to voltage converter.

The accuracy and stability of a DAC depends upon accuracy of the resistor and tracking with each other with temperature.

The disadvantage of Binary-weighted Resistor DAC are :-

1) In this wide range of resistor values are required ($2R, 2^2R, 2^3R, \dots, 2^nR$).

2) For better resolution the input word length has to be increase.

Examples for 8-bit DAC :-

1) For 8-bit DAC - resistors required are $2R, 2^2R, 2^3R, \dots, 2^7R$. The large resistor is 128 times to the smallest one.

* The Fabrication of different large resistors on IC chip is problematic.

* Voltage drop across such a large resistor due to the bias current could also effect the accuracy.

What output voltage to be produced by DAC, whose output range is 0-10V and whose input binary number is 10, 0110, 10111100

$$V_o = k V_{FS} [2^{-1}d_1 + 2^{-2}d_2 + \dots + 2^{-n}d_n]$$

$$= 1(10) [2^{-1}(1) + 2^{-2}(0)]$$

$$= 10 \left[\frac{1}{2} \right]$$

$$= 5V$$

ii) $V_0 = 10 \left[0 + \frac{1}{4} + \frac{1}{8} + 0 \right] = 10 \left[\frac{2+1}{8} \right] = 10 \times \frac{3}{8} = 3.75V$

iii) $V_0 = 10 \left[\frac{1}{2} + 0 + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + 0 + 0 \right]$
 $= 7.34V$

Calculate the value of LSB, MSB & full scale output for an 8-bit DAC for 0-10V range

$$\text{LSB} = \frac{1}{2^n}$$

$$= \frac{1}{2^8} = \frac{1}{256}$$

$$\text{MSB} = \frac{1}{2} \text{ (Full scale o/p)}$$

R-2R ladder DAC:-

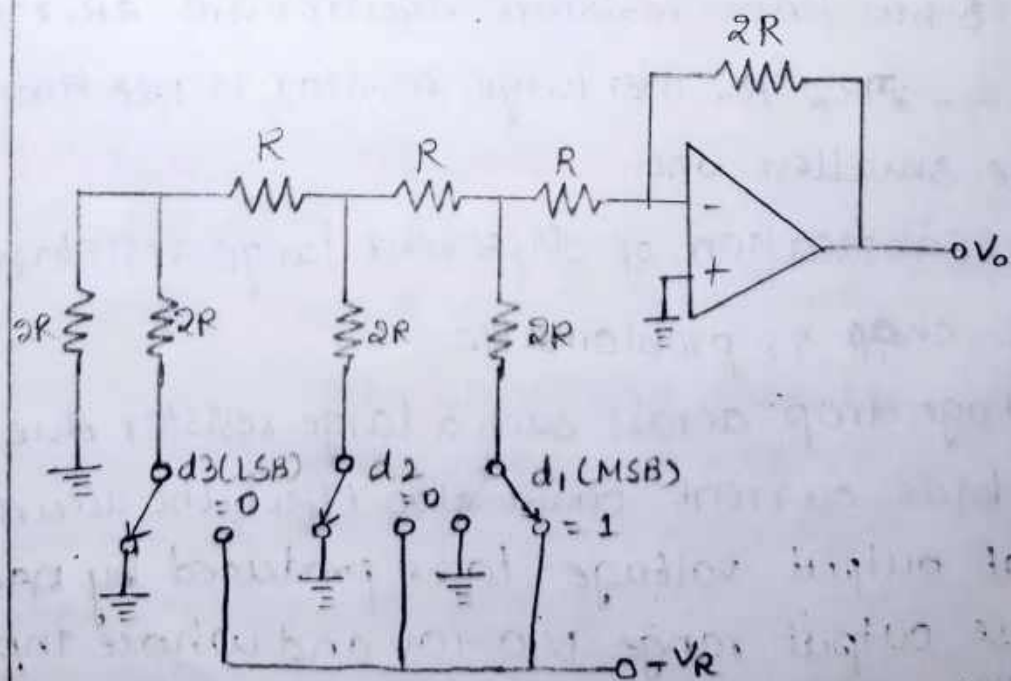
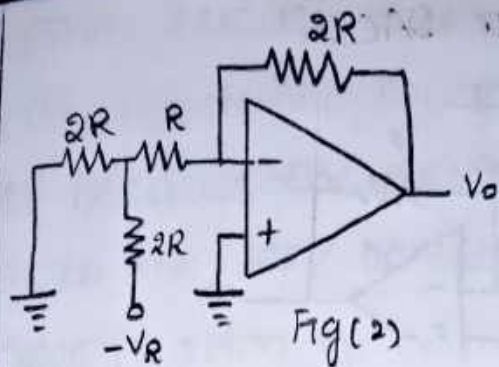
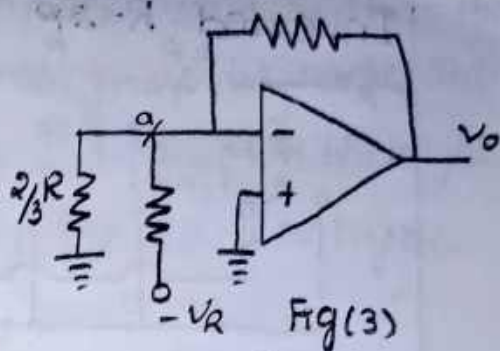


Fig 10



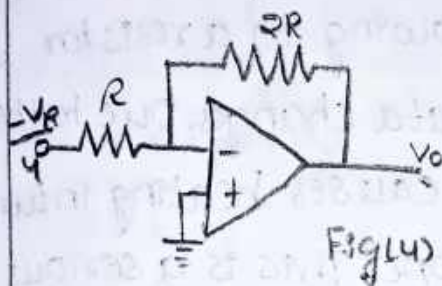
Fig(2)

$$\frac{2R \times R}{2R + R} = \frac{2R^2}{3R} = \frac{2}{3}R$$



Fig(3)

$$V_a = -V_R \times \frac{\frac{2}{3}R}{\frac{2}{3} + 2R} = -\frac{V_R}{4}$$



Fig(4)

$$V_O = -\left(-\frac{V_R}{4}\right) \times \frac{2R}{R}$$

$$V_O = \frac{V_R}{2}$$

- Wide range of resistors are required in binary weighted resistors DAC. This can be avoided by using R-2R ladder type DAC. Where only 2 types of resistors are required so it is well suited for integrated circuit realization. The typical values of R ranges from 2.5kΩ to 10kΩ.
- This circuit is a simple 3-bit DAC as shown in fig(1).
- In this if digital data = 1, SPDT switch is connected to reference voltage.
- If digital data = 0, SPDT switch is connected to ground.
- Here d₄ is the MSB bit & d₃ is the LSB.
- Here we applied the digital data is 100.

Inverted R-2R ladder DAC:-

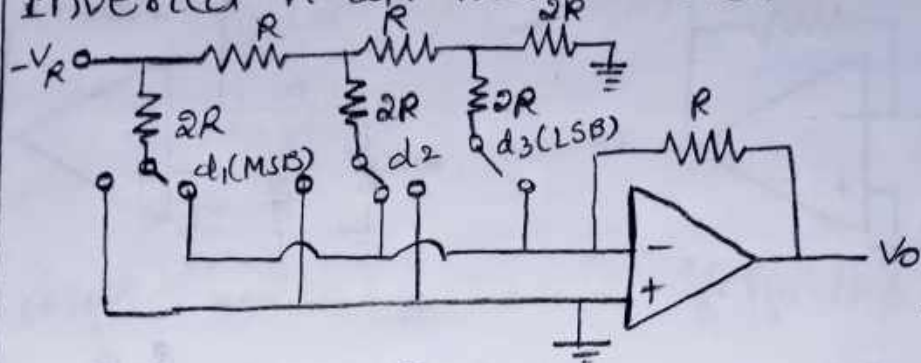


Fig: 3 bit Inverter

In weighted Resistor type DAC & R-2R ladder type DAC the current flowing in a resistor changes as the input data changes. Due to this more power dissipation causes heating in turn creates non-linearity in DAC. This is a serious problem and can be avoided completely in inverted R-2R ladder type DAC.

Here the position of MSB & LSB are interchanged. Each input binary word connects the corresponding switch either ground ($d=0$) to the inverting input terminal of the op-amp which is also at virtual ground ($d=1$). Since both the terminals of the op-amp switches d_i at the ground potential, current flowing in the resistor is constant and independent of switch position i.e., independent input binary word.

When the switch d_i at logic 0 i.e., to the left the current through $2R$ flows to the ground. When the switch d_i at logic 1 i.e., to the right the current through $2R$ sinks to the virtual ground.

The circuit has an important property that the current device equally at each of the nodes. This is because the equivalent resistance to the right or to the left of any node is exactly R .

Specification of converters:-

- 1) Resolution
- 2) Linearity
- 3) Accuracy
- 4) Monotonicity
- 5) Settling Time

Resolution:- The resolution of a converter is the smallest change in voltage which may be produced at the output (or) input of the converter.

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$$

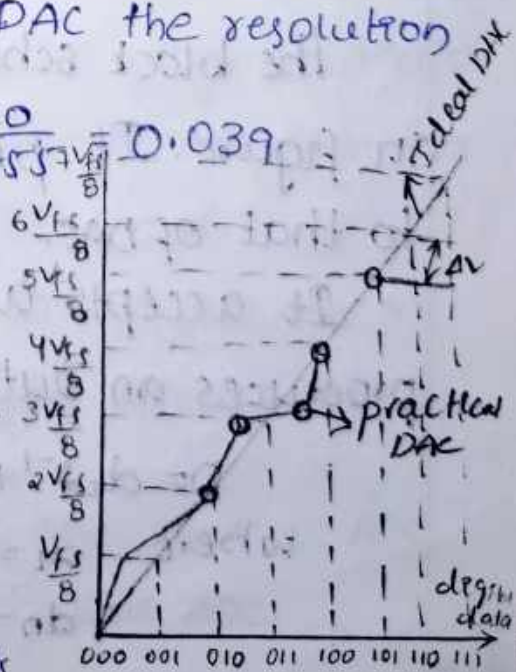
$$\begin{aligned} \text{For 8-bit DAC the resolution} &= \frac{V_{FS}}{2^8 - 1} \\ &= \frac{V_{FS}}{256 - 1} = \frac{V_{FS}}{255} \end{aligned}$$

For a 10V input 8-bit DAC the resolution

$$= \frac{V_{FS}}{255} \rightarrow \frac{10}{255} = 0.039 \text{ V}$$

Linearity:-

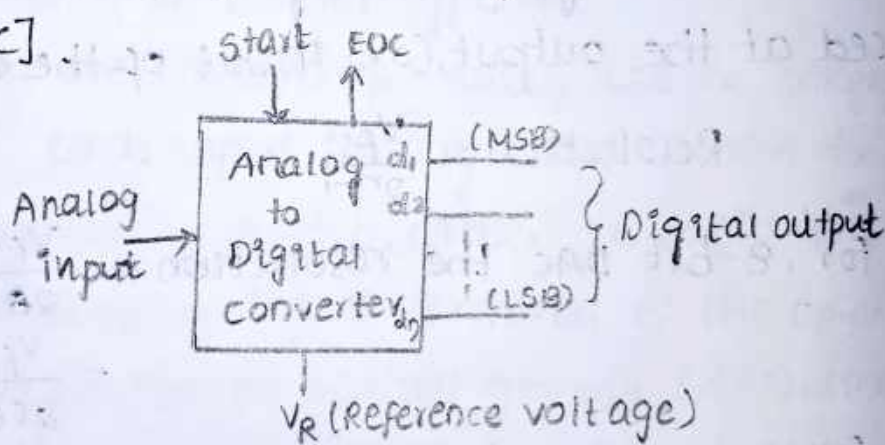
The linearity of ADC (or) DAC is an important measure of its accuracy and tells us how close the converter output is close to its



ideal transfer characteristics

- In an ideal DAC equal increment in the digital input should produce equal increment in the analog output and the transfer curve should be linear.
- However in practical DAC output voltage don't fall on a straight line because of gain & offset errors as shown in figure. By the thick line linearity error = $\frac{\epsilon}{\Delta}$
- For Good converter the linearity error is $\pm(\frac{1}{2} \text{ LSB})$.

Block diagram of Analog to Digital converter [ADC]



The block schematic of ADC is as shown in figure. It provides the function just opposite to that of DAC.

It accepts analog input voltage V_a and produces an output binary word $d_1, d_2, \dots, d_n$.

$$D = d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}$$

where $d_1 = \text{MSB}$ & $d_n = \text{LSB}$

An ADC usually has 2 additional control lines (start, EOC (End of Conversion)). The start input tells that when to start conversion, EOC output gives the information about the when the conversion is complete.

Types of ADC's:-

Direct type ADC

Indirect (Integrating) type ADC's

1) Parallel Comparator

(Flash) type ADC

1) Charge balancing ADC

2) Counter type ADC

2) Dual slope (Ramp) ADC

3) Servo tracking ADC

4) Successive Approximation ADC

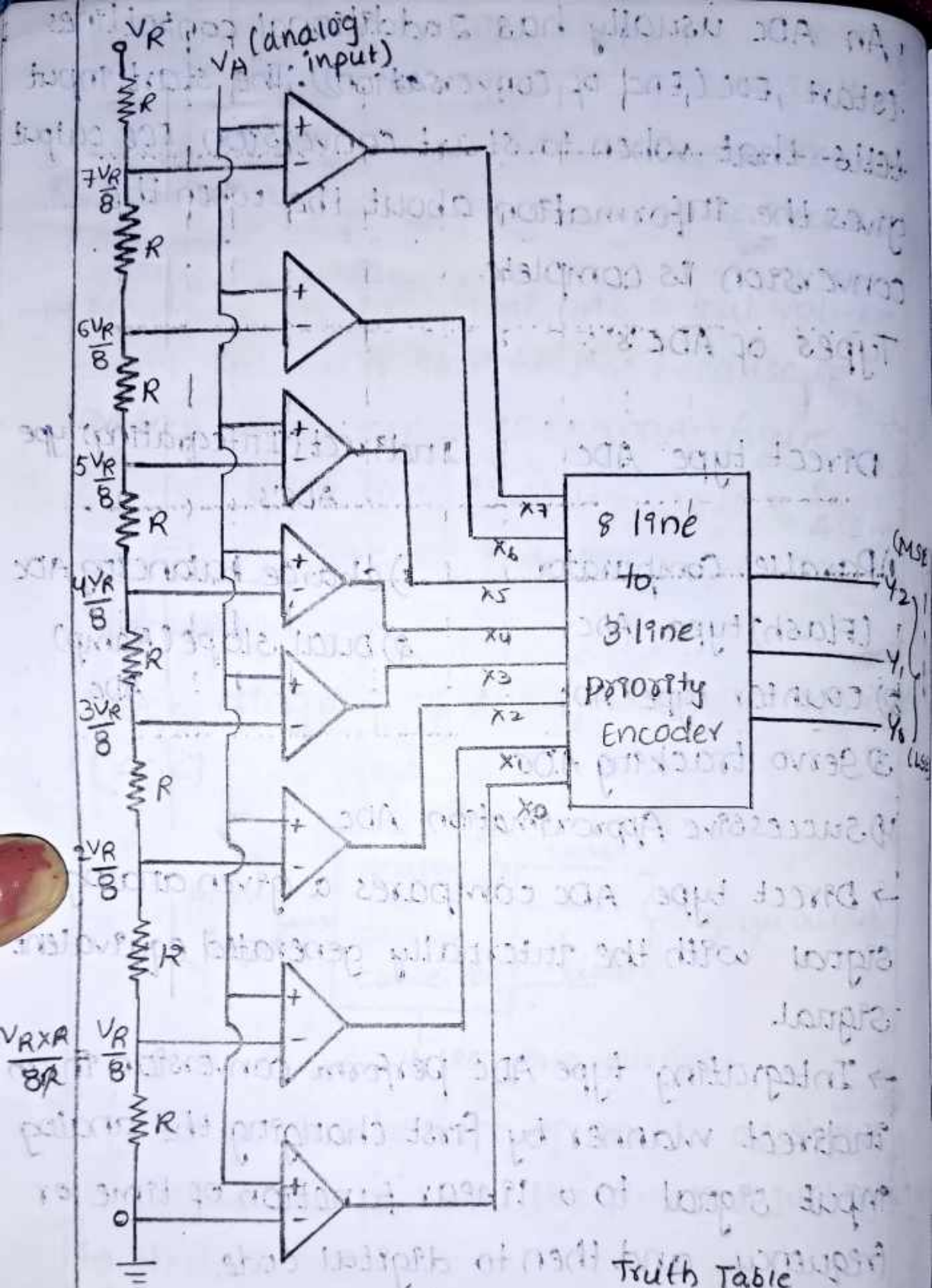
→ Direct type ADC compares a given analog signal with the internally generated equivalent signal.

→ Integrating type ADC perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to digital code.

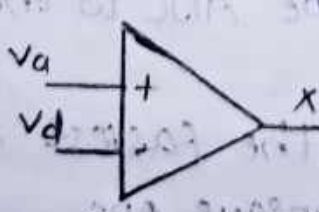
Parallel Comparator (Flash type) ADC:-

Parallel Comparator type ADC is the simplest possible ADC.

At the same time it is the fastest ADC and most expensive technique ADC.



Comparator



Truth Table

Input voltage	Logic output x
$V_a > V_d$	output of comp(x) = 1
$V_a < V_d$	o/p of comp(x) = 0
$V_a = V_d$	o/p of comp(x) = previous value

Input voltage	x_7	x_6	x_5	x_4	x_3	x_2	x_1	x_0	y_2	y_1	y_0
0 to $\frac{V_R}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8}$ to $\frac{2V_R}{8}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{2V_R}{8}$ to $\frac{3V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V_R}{8}$ to $\frac{4V_R}{8}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{4V_R}{8}$ to $\frac{5V_R}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5V_R}{8}$ to $\frac{6V_R}{8}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{6V_R}{8}$ to $\frac{7V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V_R}{8}$ to V_R	1	1	1	1	1	1	1	1	1	1	1

The circuit consists of

1. Resistive divider network

2. Op-amp Comparators

3. priority Encoder

→ At each node of resistive divider a comparison voltage is available, since all the resistors are of equal value.

→ The voltage levels available at the nodes are equally divided between the reference voltage at the ground.

→ The purpose of the circuit is to compare the analog input voltage V_a with each of the node voltages. The truth table for the flash type ADC is as shown in figure.

→ The circuit has the advantage of high

Speed as the conversion takes place simultaneously rather than sequentially.

Advantages:-

1. Conversion time 100ns or less.
2. Conversion time is limited only by the speed of comparators and the priority encoder.
3. By using advanced micro devices (AMD686A) comparator and 7147 priority encoder we can reduce conversion time to 120ns.

Disadvantages:-

The number of comparator required almost for each added bit.

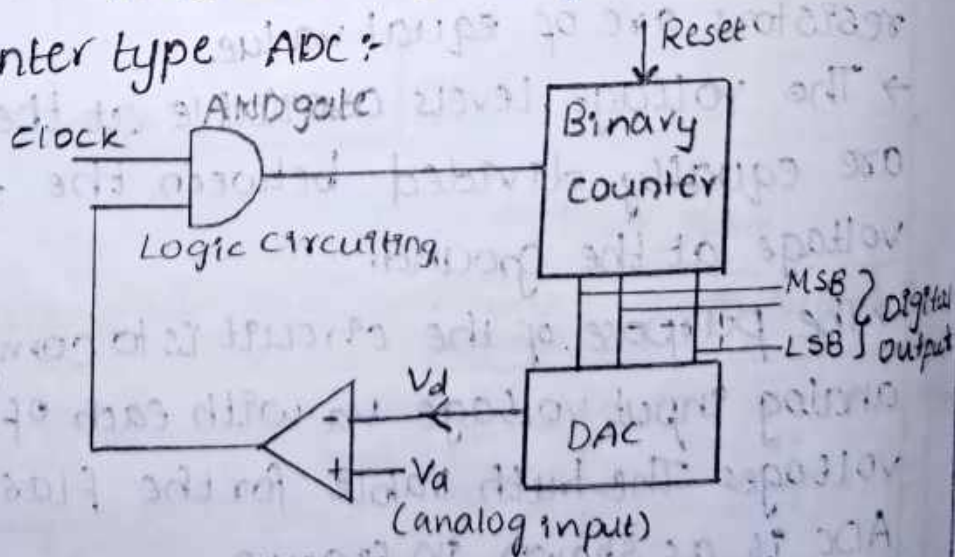
Eg:- For a 2-bit ADC

$$n=2 \rightarrow 2^n = 2^2 = 4 \text{ comparators}$$

For a 3-bit ADC

$$n=3 \rightarrow 2^3 = 8 \text{ comparators}$$

Counter type ADC:-



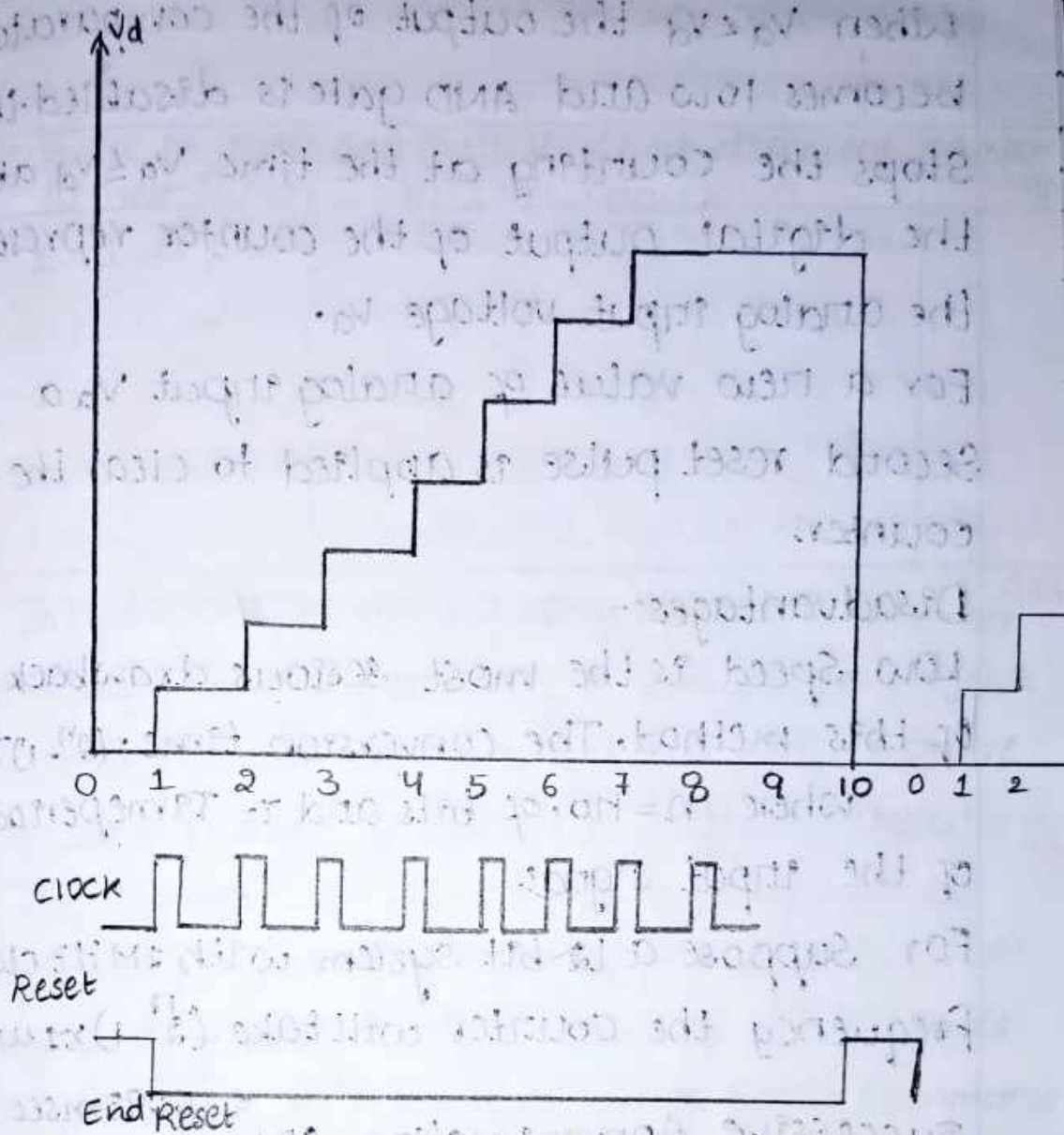


Figure shows the counter type ABC. The counter is reset to zero by applying a reset pulse. Upon release of reset (0). The clock pulses are counted by the binary counter. These clock pulses go through the AND Gate which is enable by the voltage comparator as high output. * The number of pulses counted increases with the time, the binary word representing the count is used as the 2^{nd} of DAC whose o/p is staircase of that type shown in figure.

- * The analog output V_d of the DAC is compared to the analog input V_a by the comparator.
- * If $V_a > V_d$ the o/p of the comparator becomes high & the AND gate is enabled to allow the transmission of clock pulses to the counter.

When $V_a < V_d$ the output of the comparator becomes low and AND gate is disabled this stops the counting at the time $V_a \leq V_d$ and the digital output of the counter represents the analog input voltage V_a .

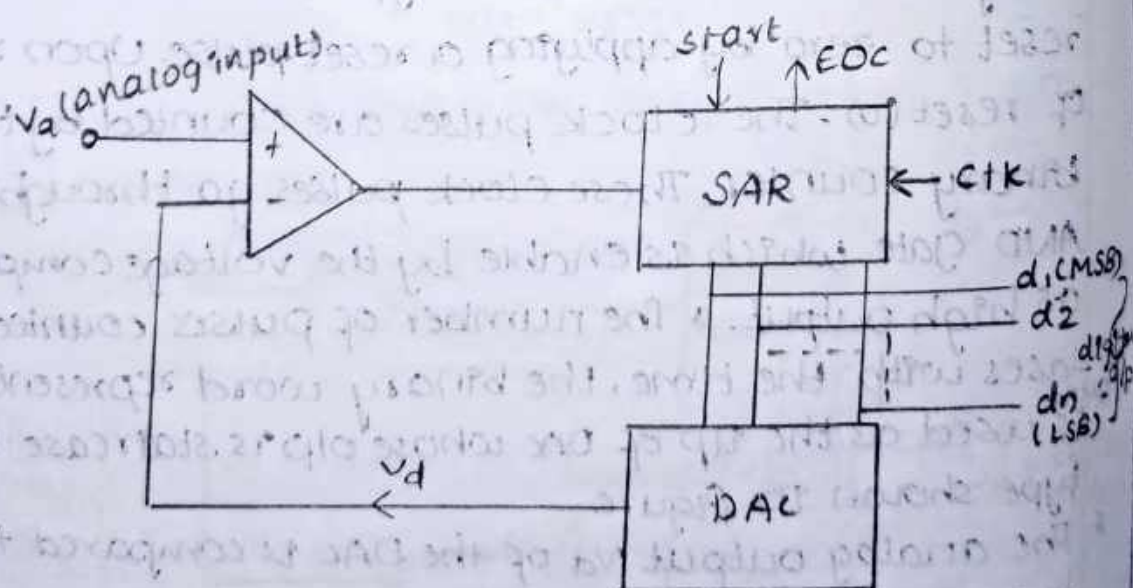
For a new value of analog input V_a a second reset pulse is applied to clear the counter.

Disadvantages:-

Low Speed is the most serious drawback of this method. The conversion time $= (2^n - 1)T$ where n = no. of bits and T = Time period of the input signal.

For Suppose a 12-bit system with 1MHz clock frequency the counter will take $(2^{12} - 1) \times 1 \mu\text{sec}$
 $= 4.095 \text{ msec}$

Successive Approximation ADC :-



Successive Approximation ADC is shown in Figure:

Convert Digital Representation	SAR Output V_d at different stages in conversion	Comparator op
1 0 1 1	1 0 0 0	1
	1 0 1 0	1
	1 0 1 1	0
	1 1 0 1	1

This technique uses a very efficient codes of ^{an} strategy to compare 'n' bit conversion in just 'n' clock pulses. For a 4-bit converter require 4 clock pulses to obtain a digital output. The circuit ^{uses} SAR [Successive Approximation Register] to find the required value of each bit by Trial & error method. The circuit operates as follows:- with the arrival of start command, The SAR sets the MSB bit = 1 with all other bits to zero, so that the trial code is 1000.

The output V_d of the DAC is now compared with analog input V_a .

If $V_a >$ the DAC output V_d then 1000 is less than the correct digital representation. The MSB is left at 1 and next lower significant bit is made 1 & further tested.

If V_a less than the DAC output V_d then 1000 is greater than the correct digital representation. So Reset MSB to '0' & go-on to the

next lower significant bit. This procedure is repeated for all subsequent bits 1 at a time, until all bit positions have been tested. Whenever the DAC output crosses V_a i.e., $V_a > V_d$ the comparator changes the state, this can be taken as EOC command.

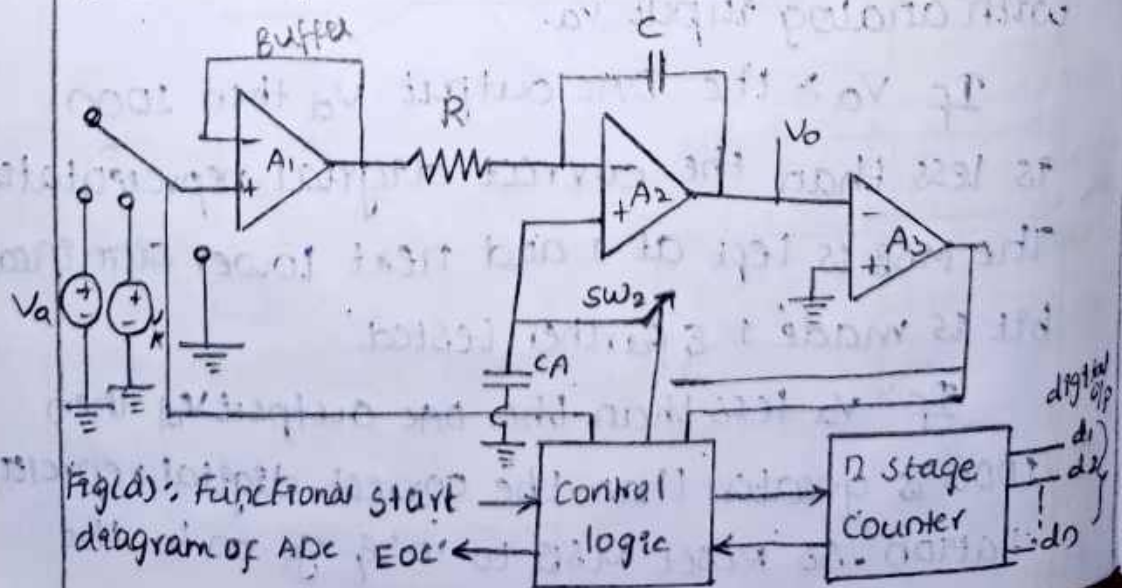
It requires four pulses to establish the accurate output regardless of the value of the analog input. However 1 additional clock pulse is used to load the output register, re-initialize the circuit. SAR is more versatile and superior to all other circuits.

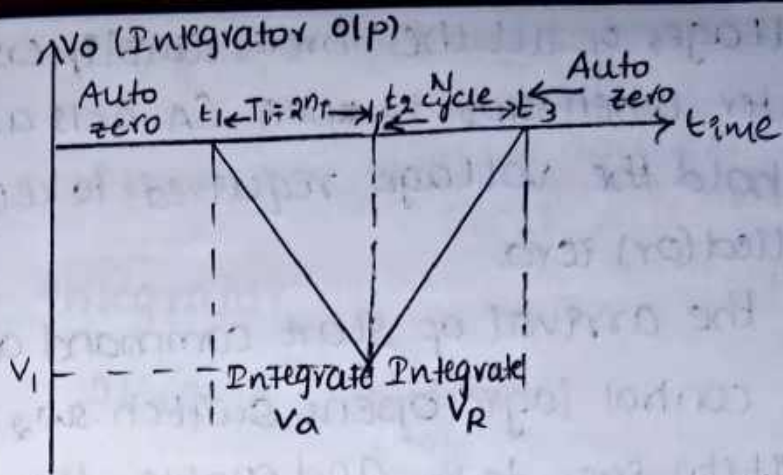
Indirect type (Integrating) ADC's:

In this ADC's first we convert analog input into a linear function of time (or) frequency and then to digital code. In this there are two types:-

- 1) charge balancing ADC
- 2) Dual slope / Dual Ramp ADC

Dual Slope ADC:-





Fig(b): Integrator output waveform for the Dual slope ADC

- The circuit consists of high impedance buffer A_1 and precision integrator A_2 and a voltage ~~to~~ comparator A_3 .
 - The converter first integrates the analog input signal for a fixed duration of 2π clock as shown in fig(b). Then it integrates an internal reference voltage V_R for opposite polarity until the integrator output is zero.
 - The N number of cycles are required to return the integrator to zero is proportional to the value of V_a average over the integration period. Hence N represents the desired output digital code.
- i) Before the start command arrives the switch SW_1 is connected to the ground and switch SW_2 is closed. Any offset voltage present in the A_1, A_2 & A_3 after the integration appears across the capacitor. The capacitor C_A thus provides automatic compensation for the input offset

voltages of all the three amplifiers.

(ii) Later when sw_2 is open CA acts as a memory to hold the voltage required to keep the offset nulled (or) zero.

(iii) At the arrival of start command at $t = t_1$ the control logic opens switch sw_2 and connects switch sw_1 to v_a and enables the counter starting from 0.

→ The circuit uses N stage ripple counter and therefore the counter reset to 0 after counting the 2^N clock pulses.

→ The analog voltage v_a is integrated for a fixed number of 2^N counts of the clock pulses after which the counter reset to 0. If the clock period is T the integration takes place a time $t_1 = 2^N T$ and shown in fig(b).

→ The counter resets itself to zero at the end of time interval t_1 & the switch sw_1 is connected to reference voltage ($-V_R$) the output voltage v_o will now has positive slope. As long as v_o is negative the output of the comparator is positive and control logic allows the clock pulses to be counted. However when v_o becomes just zero at time $t = t_3$ the control logic issues an end of conversion (EOC) command and low for the clock pulses enter into the counter.

$$T_1 = t_2 - t_1 = \frac{2^n \text{ count}}{\text{clock rate}}$$

$$V_R (t_3 - t_1) = \frac{\text{digital count } N}{\text{clock rate}}$$

for an integrator

$$\Delta V_0 = \frac{-1}{RC} V(\Delta t)$$

$$V_0 = -\frac{1}{RC} V_a (t_2 - t_1) \quad (1)$$

$$V_0 = -\frac{1}{RC} (-V_R) (t_2 - t_3) \quad (2)$$

$$V_a (t_2 - t_1) = -V_R (t_2 - t_3)$$

$$\text{where } (t_2 - t_1) = \frac{2^n}{C \cdot R}$$

$$(t_3 - t_1) = \frac{N}{C \cdot R}$$

$$V_a 2^n = V_R N$$

$$V_a = \frac{V_R N}{2^n}$$

Here analog input is directly proportional to N and is independent of RC product and T .

Advantage:-

*Excellent Noise Rejection

Disadvantage:-

*It takes a long conversion time i.e. approximately 20msec.

Applications:-

*It is used for accurate measurement of slowly varying signals such as thermocouples and weighing scales.

* In digital panel meter.

* In Multimeters

If the analog signal V_a is 4.129V. Find the equivalent digital number ($n=16$, $V_R=8V$)

$$V_a = 4.129V$$

$$(n=16, V_R=8V)$$

$$V_a = \frac{V_R N}{2^n}$$

$$N = \frac{V_a \times 2^n}{V_R}$$

$$N = \frac{4.129 \times 2^{16}}{8}$$

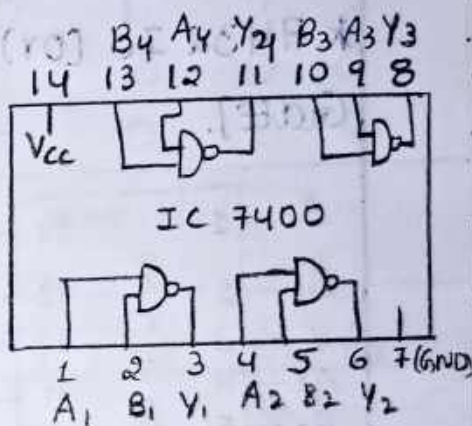
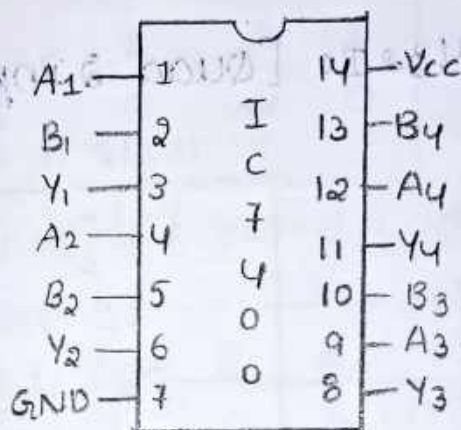
$$N = 33,825$$

IV. COMBINATIONAL LOGIC IC'S

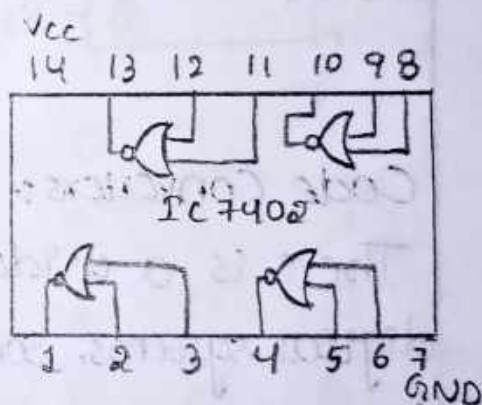
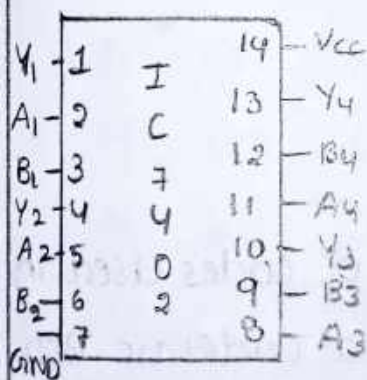
Logic Gates:-

1. Basic Gates :- AND, OR, NOT
2. Universal Gates :- NAND, NOR
3. Exclusive gates :- EX-OR, EX-NOR

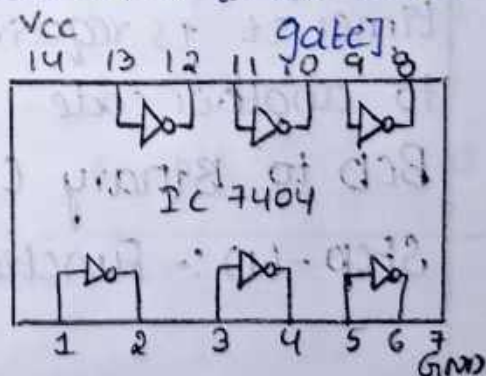
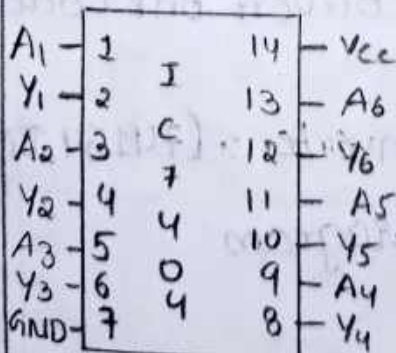
* For NAND Gate we use 7400 IC (or) 7401 IC
[Quad 2 Input NAND Gate]



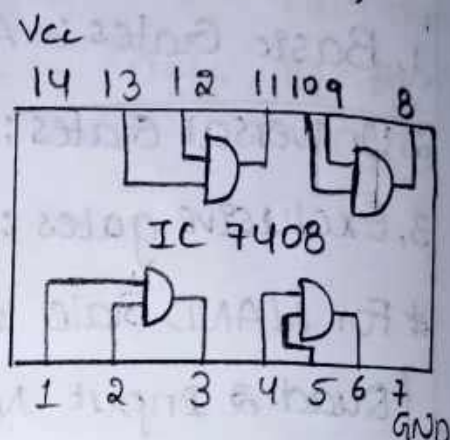
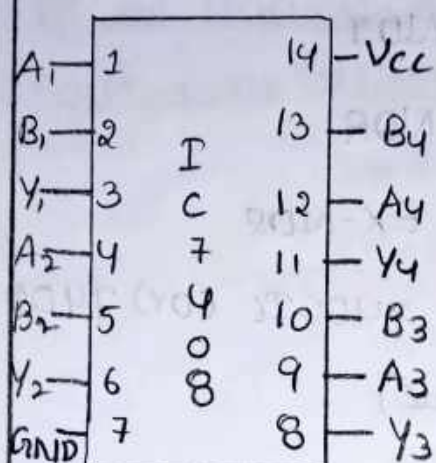
* 7402 IC (or) 5402 IC [Quad 2 Input NOR gate]



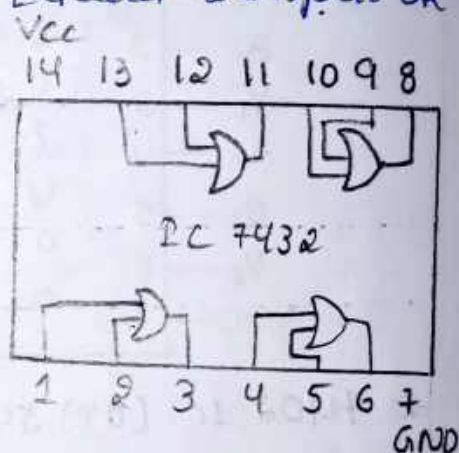
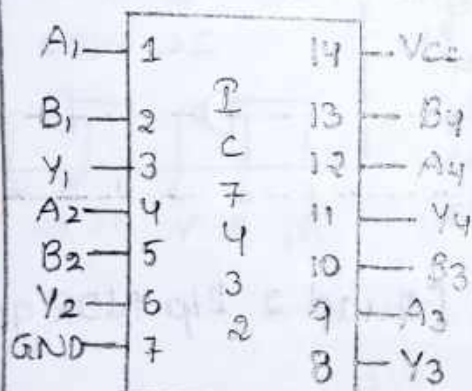
* NOT Gate: IC 7404 (or) 5404 IC [Hex inverting gate]



* 7408 IC (or) 5408 IC [Quad 2 Input AND gate.



* 7432 IC (or) 5432 IC [Quad 2 Input OR Gate].



Code Converters:-

There is a wide variety of codes used in digital systems. Some of these codes are BCD, Binary, Excess-3, Gray code, etc. --- Many times it is required to convert one code to another code.

BCD to Binary Code Converter:- (74184 IC)

Step-1:- Functional diagram

BCD				Binary			
B ₃	B ₂	B ₁	B ₀	D	C	B	A
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1

BCD to Excess-3 Code Converter:

B ₃	B ₂	B ₁	B ₀	E ₃	E ₂	E ₁	E ₀
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Step-2:- K-Map Simplification

E₀:-

	$\bar{B}_1\bar{B}_0$	$\bar{B}_1B_0$	$B_1\bar{B}_0$	B_1B_0
$\bar{B}_3\bar{B}_2$	1	0	0	1
$\bar{B}_3B_2$	1	0	0	1
$B_3\bar{B}_2$	X	X	X	X
B_3B_2	1	0	X	X

$$E_0 = \bar{B}_0$$

E₁:-

	$\bar{B}_1\bar{B}_0$	$\bar{B}_1B_0$	$B_1\bar{B}_0$	B_1B_0
$\bar{B}_3\bar{B}_2$	1	0	1	0
$\bar{B}_3B_2$	1	0	1	0
$B_3\bar{B}_2$	X	X	X	X
B_3B_2	1	0	X	X

$$E_1 = \bar{B}_1\bar{B}_0 + B_1\bar{B}_0 = \bar{B}_1$$

E₂:-

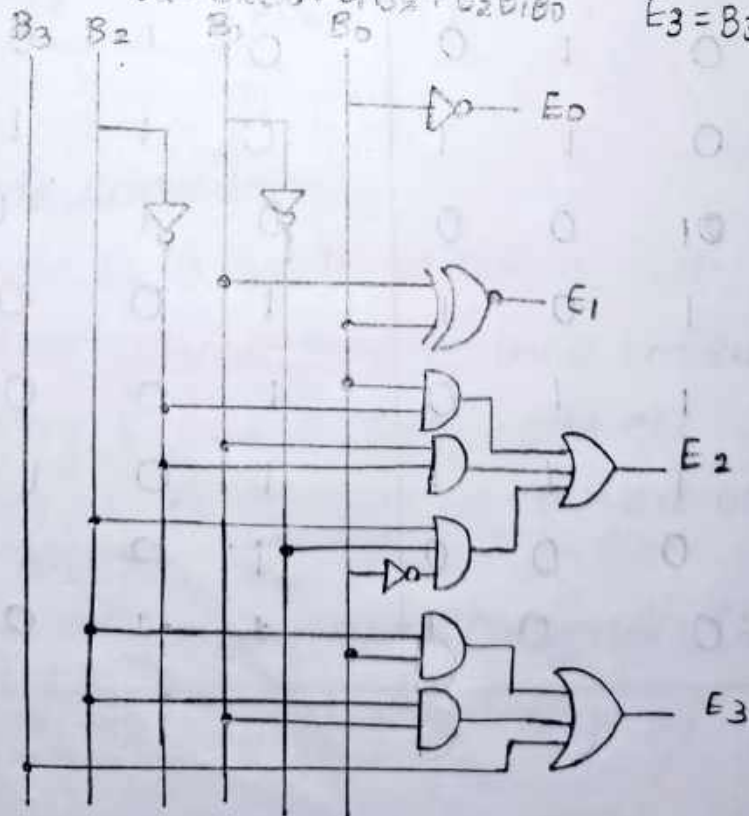
	$\bar{B}_1\bar{B}_0$	$\bar{B}_1B_0$	$B_1\bar{B}_0$	B_1B_0
$\bar{B}_3\bar{B}_2$	0	1	1	1
$\bar{B}_3B_2$	1	0	0	0
$B_3\bar{B}_2$	X	X	X	X
B_3B_2	0	1	X	X

$$E_2 = \bar{B}_2\bar{B}_0 + B_1\bar{B}_2 + B_2\bar{B}_1\bar{B}_0$$

E₃:-

	$\bar{B}_1\bar{B}_0$	$\bar{B}_1B_0$	$B_1\bar{B}_0$	B_1B_0
$\bar{B}_3\bar{B}_2$	0	0	0	0
$\bar{B}_3B_2$	0	1	1	1
$B_3\bar{B}_2$	X	X	X	X
B_3B_2	1	1	X	X

$$E_3 = B_3 + B_0B_2 + B_2B_1$$



Design a 4-bit Binary to Gray Code Converter

4-bit Binary code = $B_3 B_2 B_1 B_0$

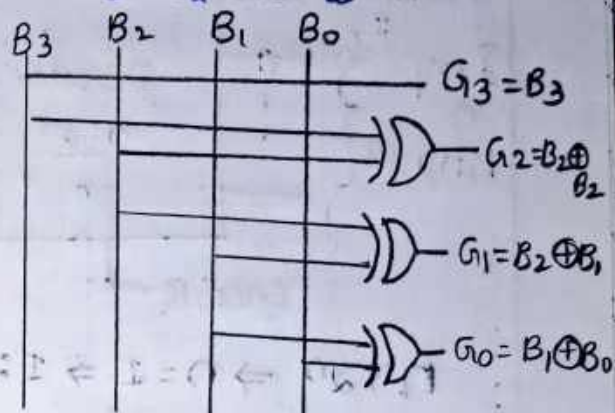
Gray code = $G_3 G_2 G_1 G_0$

$$G_3 = B_3$$

$$G_2 = B_3 \oplus B_2$$

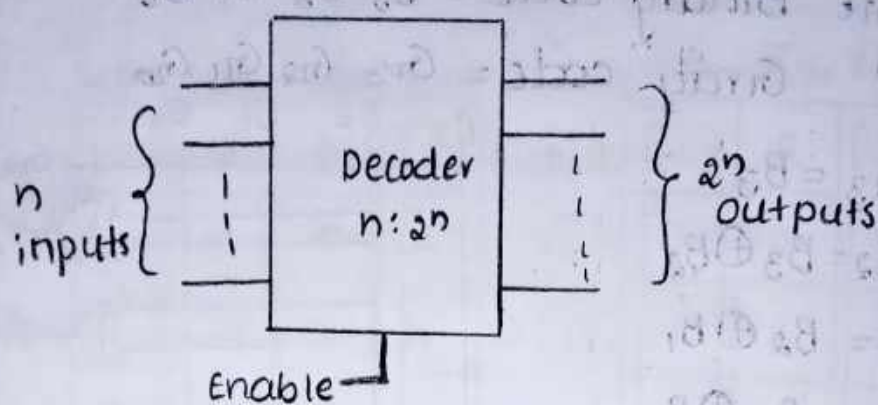
$$G_1 = B_2 \oplus B_1$$

$$G_0 = B_1 \oplus B_0$$



Binary code				Gray Code			
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Decoder:

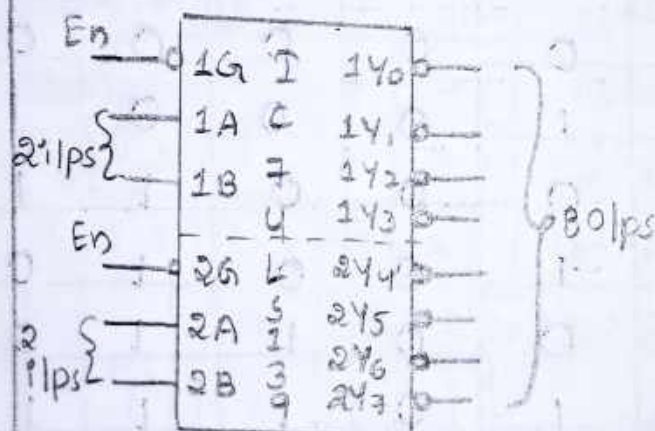


$$n:2^n \Rightarrow n=1 \Rightarrow 1:2$$

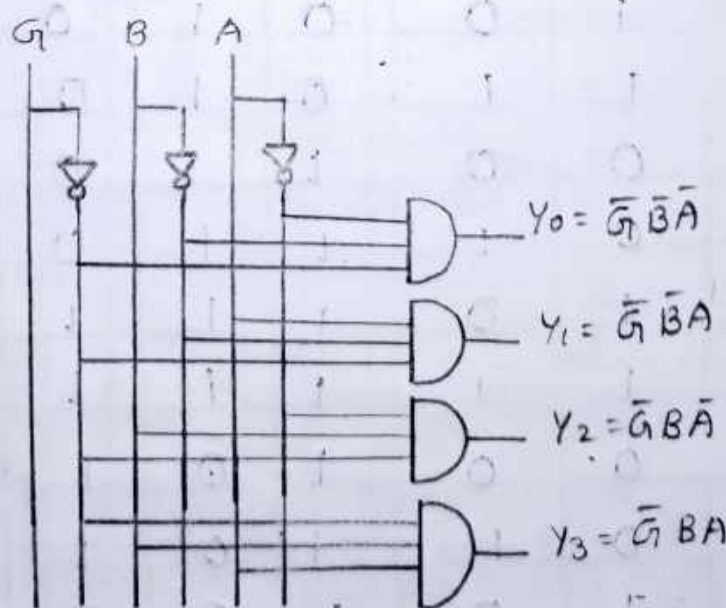
$$n=2 \Rightarrow 2:4$$

$$n=3 \Rightarrow 3:8$$

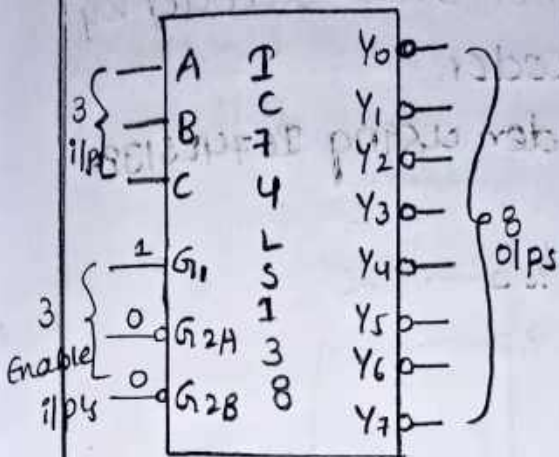
IC 74LS139 (Dual 2:4 decoder):



G	B	A	$\bar{Y}_3$	$\bar{Y}_2$	$\bar{Y}_1$	$\bar{Y}_0$
1	X	X	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1



IC 74LS138 (3 to 8 Decoder):



Logic symbol

Functional Table:-

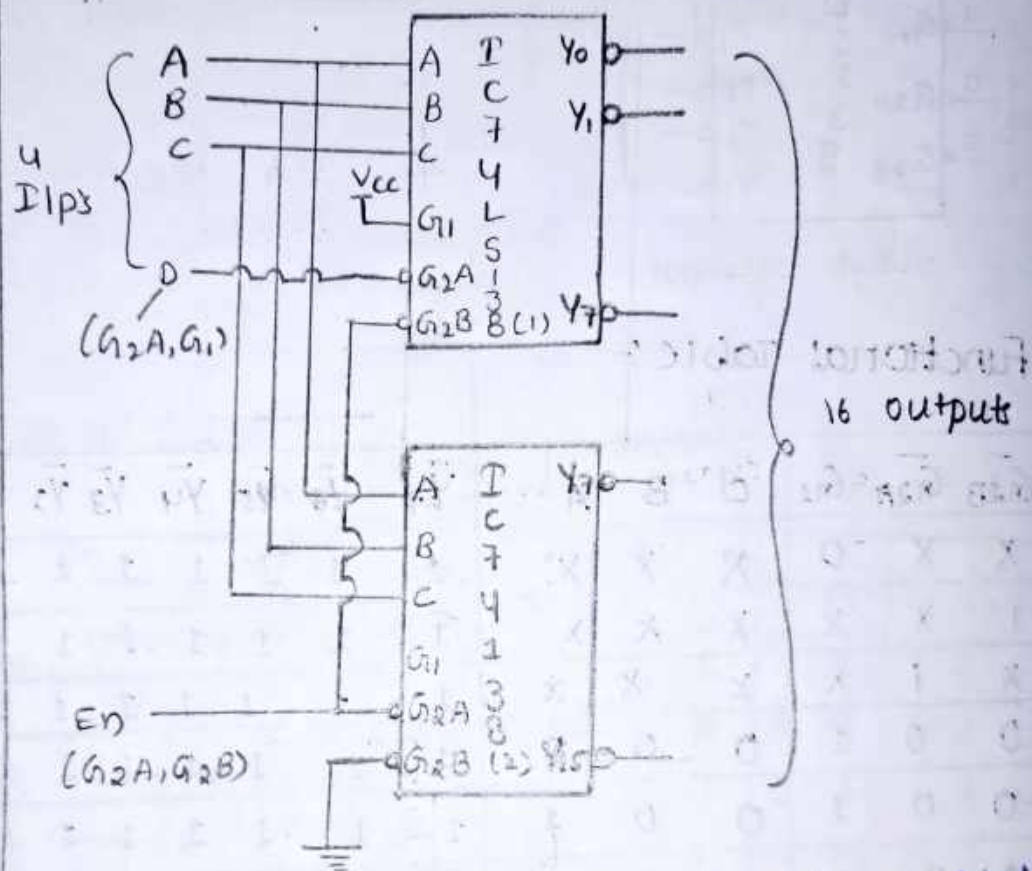
$\overline{G_{2B}}$	$\overline{G_{2A}}$	G_1	C	B	A	$\overline{Y_7}$	$\overline{Y_6}$	$\overline{Y_5}$	$\overline{Y_4}$	$\overline{Y_3}$	$\overline{Y_2}$	$\overline{Y_1}$	$\overline{Y_0}$
X	X	0	X	X	X	1	1	1	1	1	1	1	1
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	1	1	1	1	1	1	0	0
0	0	1	0	0	1	1	1	1	1	1	0	1	0
0	0	1	0	1	0	1	1	1	1	0	1	1	0
0	0	1	0	1	1	1	1	1	0	1	1	1	0
0	0	1	1	0	0	1	1	1	0	1	1	1	1
0	0	1	1	0	1	1	1	0	1	1	1	1	1
0	0	1	1	1	0	1	0	1	1	1	1	1	1
0	0	1	1	1	1	0	1	1	1	1	1	1	1

* The 74LS138 is a 3 to 8 decoder. It has active high 3 inputs & 3 enable inputs, G_1 - Active low, G_{2A}, G_{2B} - Active high and all outputs are active low outputs from Y_0 to Y_7 .

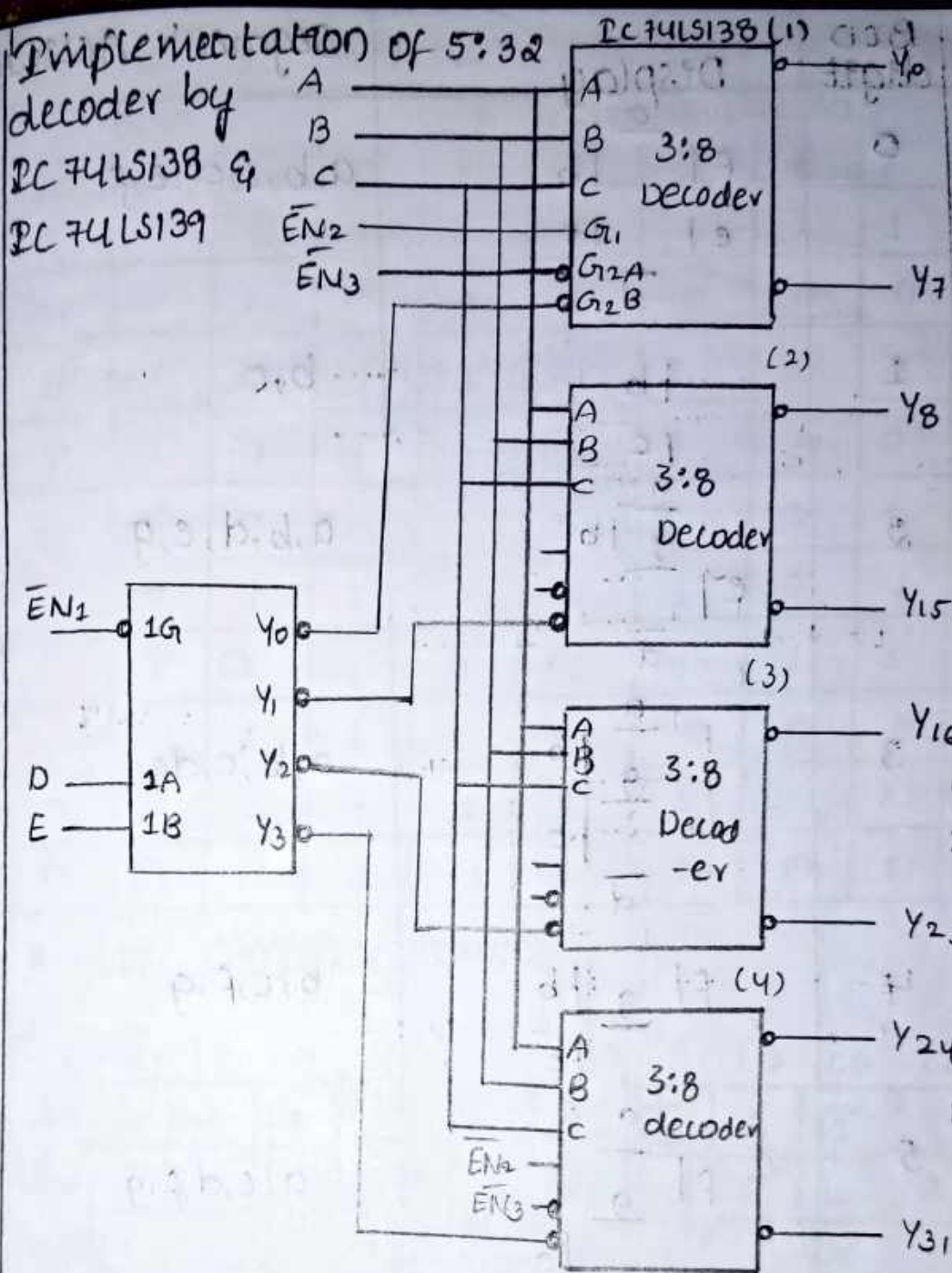
Cascading of Binary decoder:

Implementation of higher order decoder by using lower order decoder.

Implement 4:16 decoder using IC 74LS138.



- * In this one input line D is used to enable/disable the decoder.
- * When $d=0$ the top decoder is enabled and otherwise one is disabled. Thus, the bottom decoder outputs are all 1s and the top 8 outputs, depending upon the inputs we get $Y_0, \dots, Y_7$ outputs.
- * When $d=1$ the top decoder must be disabled and bottom decoder must be enabled. The top decoder outputs are all 1s & the bottom 8 outputs are depending upon the inputs we get $Y_8, \dots, Y_{15}$ outputs.



Design BCD to 7-segment Display Decoder

The application of 7-segment display is used to give visual indication of the output states of the digital IC's such as decoders, counters, latches etc.---

* IC 7449 is used.

BCD digit	Display	Segments Activated
0	$ \begin{array}{c} \overline{a} \\ f \quad b \\ e \quad c \\ \overline{d} \end{array} $	a, b, c, d, e, f
1	$ \begin{array}{c} b \\ c \\ \overline{a} \\ \overline{g} b \\ e \quad c \\ \overline{d} \end{array} $	b, c
2	$ \begin{array}{c} \overline{a} \\ \overline{g} b \\ e \quad c \\ \overline{d} \end{array} $	a, b, d, e, g
3	$ \begin{array}{c} \overline{a} \\ \overline{g} b \\ c \\ \overline{d} \end{array} $	a, b, c, d, g
4	$ \begin{array}{c} f \quad b \\ \overline{g} c \\ \overline{a} \\ f \quad b \\ \overline{g} c \\ c \\ \overline{d} \end{array} $	b, c, f, g
5	$ \begin{array}{c} \overline{a} \\ f \quad b \\ \overline{g} c \\ c \\ \overline{d} \end{array} $	a, c, d, f, g
6	$ \begin{array}{c} f \quad b \\ \overline{g} c \\ e \quad c \\ \overline{d} \\ \overline{a} \\ b \\ c \\ \overline{a} \\ f \quad b \\ \overline{g} c \\ c \\ \overline{d} \end{array} $	a, c, d, e, f, g
7	$ \begin{array}{c} \overline{a} \\ b \\ c \\ \overline{a} \\ f \quad b \\ \overline{g} c \\ c \\ \overline{d} \end{array} $	a, b, c
8	$ \begin{array}{c} \overline{a} \\ f \quad b \\ \overline{g} c \\ e \quad c \\ \overline{d} \\ \overline{a} \\ f \quad b \\ \overline{g} c \\ c \\ \overline{d} \end{array} $	a, b, c, d, e, f, g
9	$ \begin{array}{c} \overline{a} \\ f \quad b \\ \overline{g} c \\ c \\ \overline{d} \end{array} $	a, b, c, d, f, g

Functional Table :-

BCD				7-segment Display						
A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

K-Map Simplification:-

a:-

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	1	1
$\bar{A}B$	0	1	1	1
AB	X	X	X	X
$A\bar{B}$	1	1	X	X

$\rightarrow C$
 $\rightarrow BD$
 $\rightarrow \bar{B}\bar{D}$
 $\vee A$

$$a = A + C + BD + \bar{B}\bar{D}$$

$$= A + C + B \odot D$$

c:-

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	1	0
$\bar{A}B$	1	1	1	1
AB	X	X	X	X
$A\bar{B}$	1	1	X	X

$\rightarrow B$
 $\rightarrow \bar{C}$
 $\rightarrow D$

$$c = \bar{C} + D + B$$

b:-

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	1	1
$\bar{A}B$	1	0	1	0
AB	X	X	X	X
$A\bar{B}$	1	1	X	X

$$b = \bar{B} + \bar{D}\bar{C} + CD$$

$$= \bar{B} + (C \odot D)$$

d:-

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	1	1
$\bar{A}B$	0	1	0	1
AB	X	X	X	X
$A\bar{B}$	1	1	X	X

$$d = \bar{B}\bar{D} + A + C\bar{D} + \bar{B}C + B\bar{C}D$$

e:-

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 1	1 0	3 0	2 1
$\bar{A}B$	4 0	5 0	7 0	6 1
AB	12 X	13 X	15 X	14 X
$A\bar{B}$	8 1	9 0	11 X	10 X

$$e = C\bar{D} + B\bar{D}$$

f:-

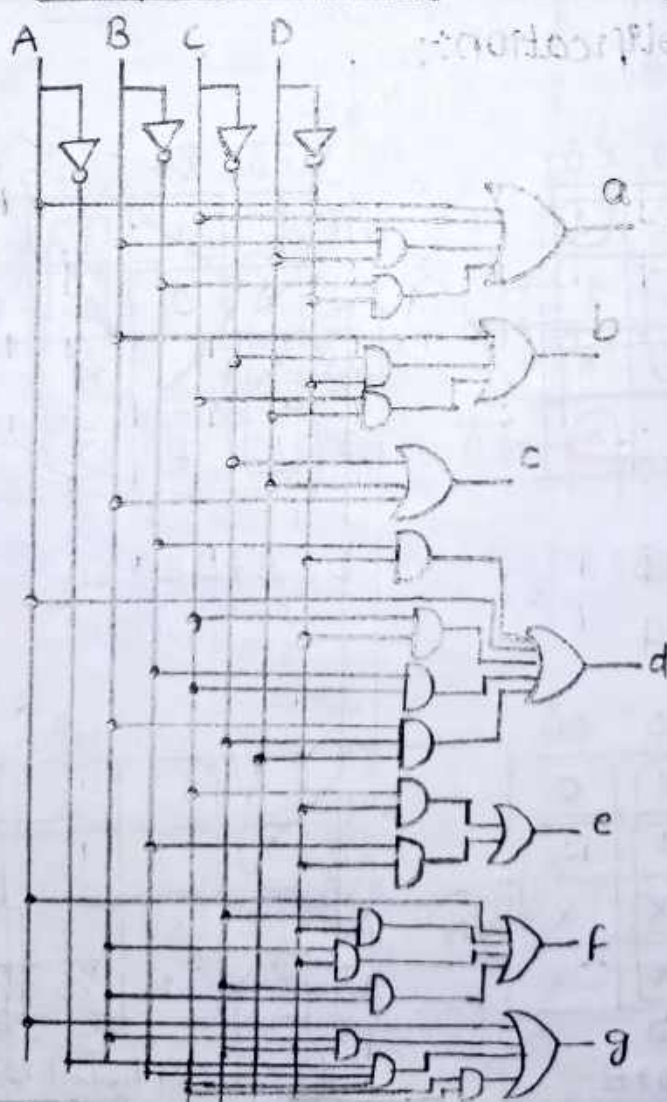
	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	0	0
$\bar{A}B$	1	1	0	1
AB	X	X	X	X
$A\bar{B}$	1	1	X	X

$$f = A + \bar{C}\bar{D} + B\bar{D} + \bar{C}B$$

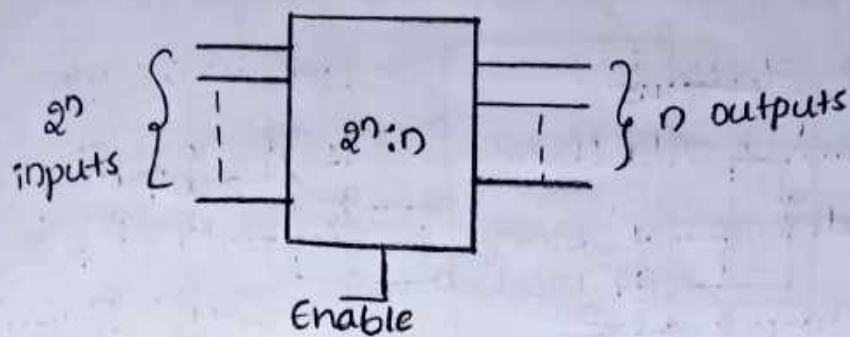
g:-

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 0	1 0	3 1	2 1
$\bar{A}B$	4 1	5 1	7 0	6 1
AB	12 X	13 X	15 X	14 X
$A\bar{B}$	8 1	9 1	11 X	10 X

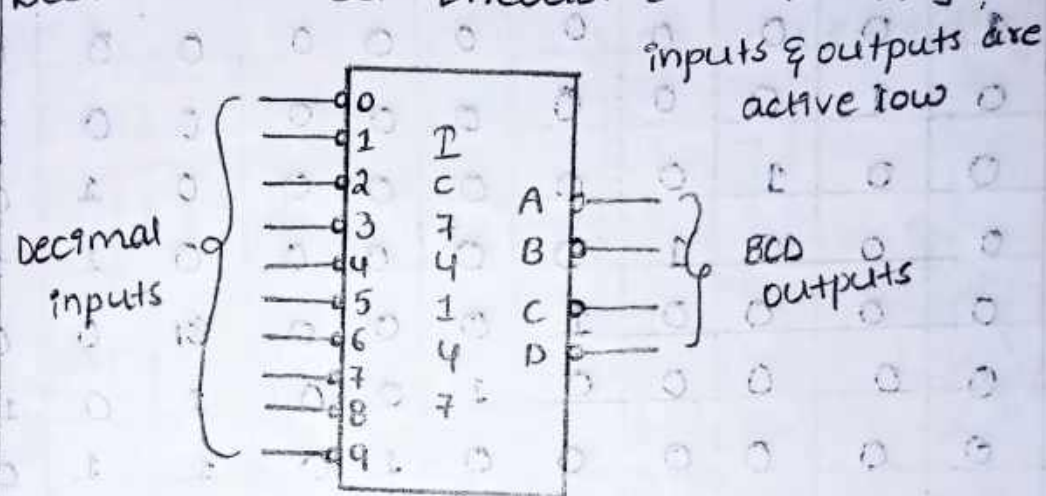
$$g = A + B\bar{C} + \bar{A}\bar{B}C + C\bar{D}$$



Encoder :-

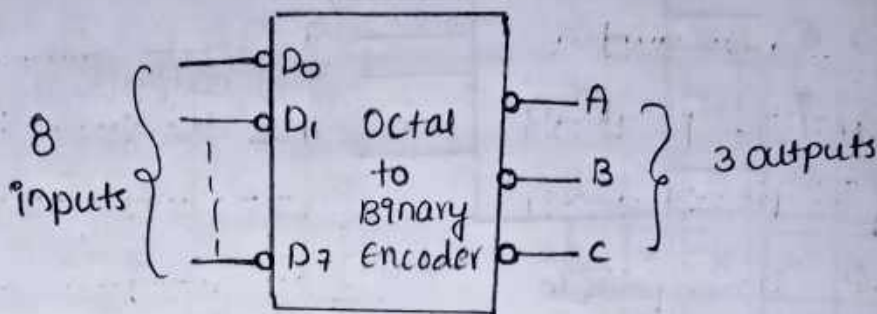


General Block diagram of Encoder Decimal to BCD Encoder [IC 74XX147]



Decimal value	0	1	2	3	4	5	6	7	8	9	D	C	B	A
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1	0
2	1	1	0	1	1	1	1	1	1	1	1	1	0	1
3	1	1	1	0	1	1	1	1	1	1	1	1	0	0
4	1	1	1	1	0	1	1	1	1	1	1	0	1	1
5	1	1	1	1	1	0	1	1	1	1	1	0	1	0
6	1	1	1	1	1	1	0	1	1	1	1	0	0	1
7	1	1	1	1	1	1	1	0	1	1	1	0	0	0
8	1	1	1	1	1	1	1	1	0	1	0	1	1	1
9	1	1	1	1	1	1	1	1	1	0	0	1	1	1

Octal to Binary Encoder:-



D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	Binary outputs		
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Priority Encoder [IC 74LS148]

It is an encoder circuit that includes priority function. In a priority encoder if two or more inputs are equal to '1' at the same time the input having the highest priority will taken output. Step-1: Functional Table:-

Inputs				Outputs		V (priority)
D ₀	D ₁	D ₂	D ₃	Y ₁	Y ₀	
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

Step-2:- K-Map Simplification

V

	$\bar{D}_2\bar{D}_3$	$\bar{D}_2D_3$	$D_2\bar{D}_3$	D_2D_3
$\bar{D}_0\bar{D}_1$	0	1	1	1
$\bar{D}_0D_1$	1	1	1	1
$D_0\bar{D}_1$	1	1	1	1
D_0D_1	1	1	1	1

$$V = D_0 + D_2 + D_3 + D_1$$

Y_0

	$\bar{D}_2\bar{D}_3$	$\bar{D}_2D_3$	$D_2\bar{D}_3$	D_2D_3
$\bar{D}_0\bar{D}_1$	X	1	1	0
$\bar{D}_0D_1$	1	1	1	0
$D_0\bar{D}_1$	1	1	1	0
D_0D_1	0	1	1	0

$\rightarrow P_1, \bar{D}_2$
 $\rightarrow D_3$

$$Y_0 = P_3 + D_1D_2$$

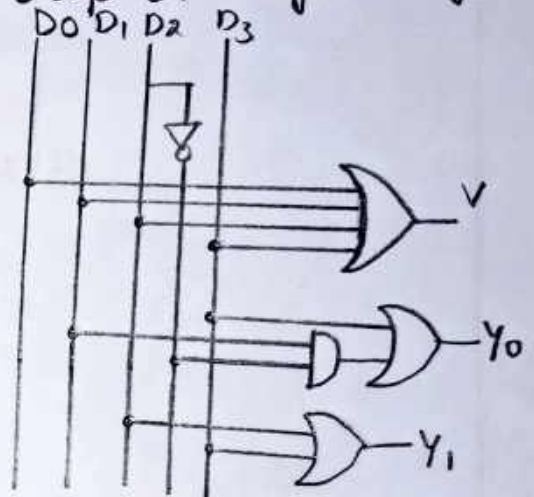
Y_1

	$\bar{D}_2\bar{D}_3$	$\bar{D}_2D_3$	$D_2\bar{D}_3$	D_2D_3
$\bar{D}_0\bar{D}_1$	X	1	1	1
$\bar{D}_0D_1$	0	1	1	1
$D_0\bar{D}_1$	0	1	1	1
D_0D_1	0	1	1	1

$\rightarrow D_2$
 $\downarrow D_3$

$$Y = D_2 + D_3$$

Step-3:- Logic diagram



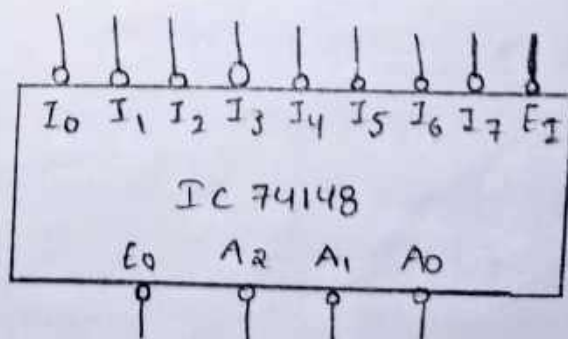
74LS148

* It is an 8-bit priority encoder.

* 8 inputs are active low and three outputs are active low.

* I_0 has the least priority and it is given as [000] I_7 has the highest priority [111].

8-bit priority Encoder:-

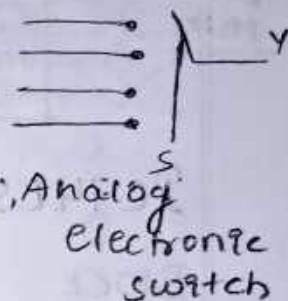


$\bar{E}_I$ is the active low enable input. The high on the $\bar{E}_I$ will force all the outputs to the inactive states. To enable active low signal that can be used to cascade of several priority encoders. [Implementation of highest / large priority encoder by using small priority encoder].

Multiplexer:-

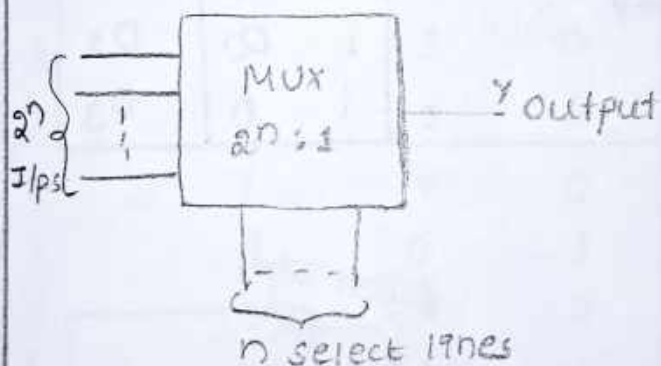
Multiplexer is a digital electronic switch it allows digital information from several sources to be routed on to a single output line.

The basic MUX has several data input lines and a single output line. The selection of particular input line is controlled by a set of selection lines.



MUX is a "many to one" and it provides a digital equivalent of analog selector switch.

Types:



$$n=1 \Rightarrow 2:1 (74LS154)$$

Quad 2:1 MUX

$$n=2 \Rightarrow 4:1 (74LS153)$$

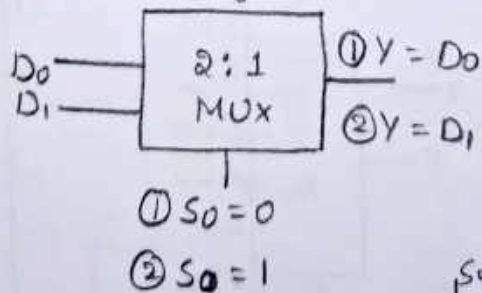
Dual 4:1 MUX

$$n=3 \Rightarrow 8:1 (74LS151)$$

$$n=4 \Rightarrow 16:1 (74LS150)$$

74LS157 (Quad 2:1 MUX)

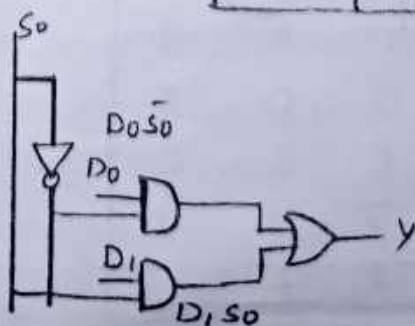
Block diagram:-



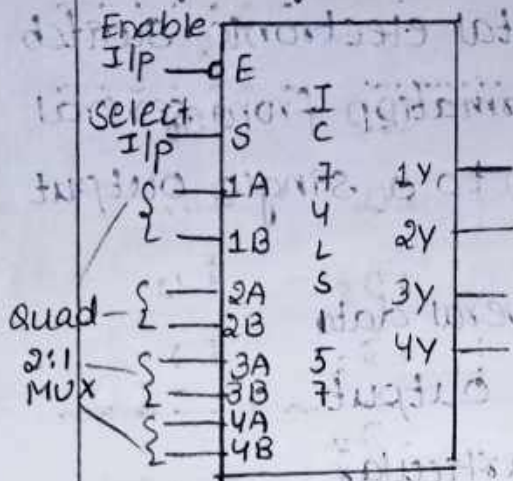
Functional Table:-

S_0	Y
0	D_0
1	D_1

Logic Diagram:-



Logic Symbol:-

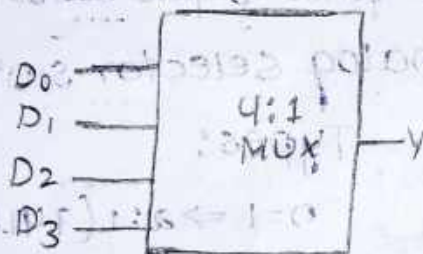


Truth Table:-

Inputs		Outputs			
E	S	1Y	2Y	3Y	4Y
1	X	0	0	0	0
0	0	1A	2A	3A	4A
0	1	1B	2B	3B	4B

IC 74LS153 (Dual 4:1 MUX):-

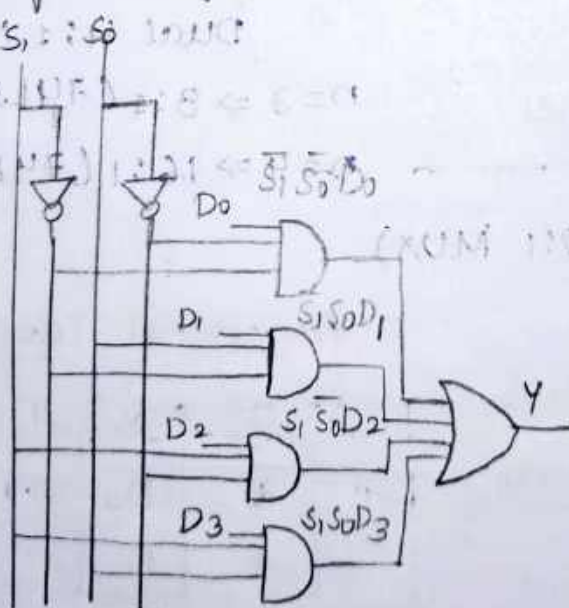
Block diagram:-



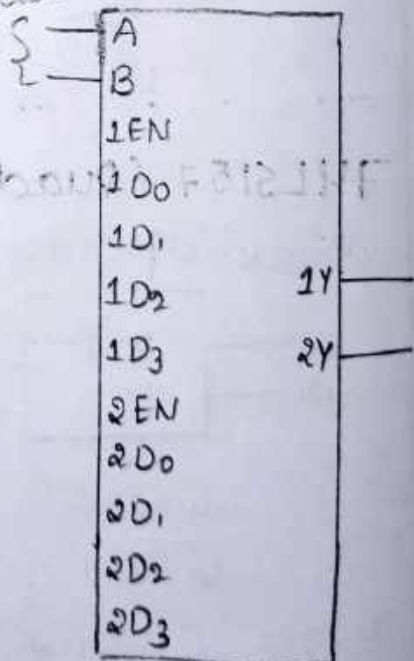
Truth Table:-

S ₁	S ₀	Y
0	0	D ₀
0	1	D ₁
1	0	D ₂
1	1	D ₃

Logic Diagram:-



Select I/Ps

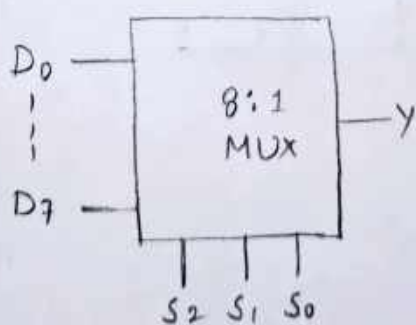


Inputs				Outputs	
1EN	2EN	B	A	1Y	2Y
0	0	0	0	1D ₀	2D ₀
0	0	0	1	1D ₁	2D ₁
0	0	1	0	1D ₂	2D ₂
0	0	1	1	1D ₃	2D ₃
0	1	0	0	1D ₀	0
0	1	0	1	1D ₁	0
0	1	1	0	1D ₂	0
0	1	1	1	1D ₃	0
1	0	0	0	0	2D ₀
1	0	0	1	0	2D ₁
1	0	1	0	0	2D ₂
1	0	1	1	0	2D ₃
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0

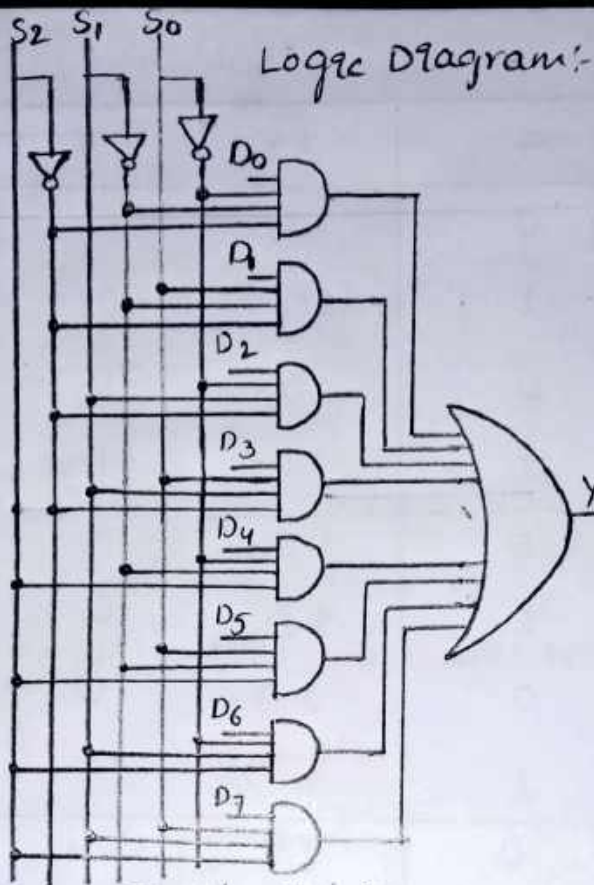
74LS151 (8:1 MUX)

Truth Table :-

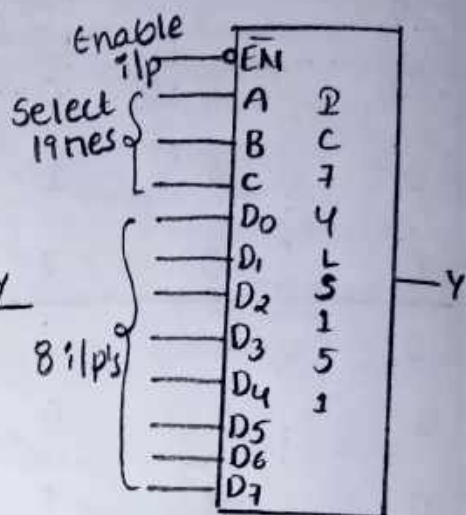
Block Diagram:-



S ₂	S ₁	S ₀	Y
0	0	0	D ₀
0	0	1	D ₁
0	1	0	D ₂
0	1	1	D ₃
1	0	0	D ₄
1	0	1	D ₅
1	1	0	D ₆
1	1	1	D ₇



Logic symbol

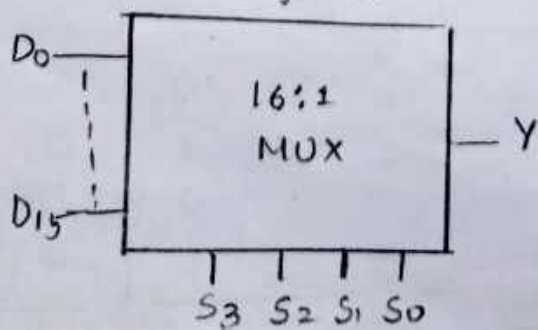


Truth Table

C	B	A	$\bar{EN}$	o/p(Y)
x	x	x	1	1
0	0	0	0	$\bar{D}_0$
0	0	1	0	$\bar{D}_1$
0	1	0	0	$\bar{D}_2$
0	1	1	0	$\bar{D}_3$
1	0	0	0	$\bar{D}_4$
1	0	1	0	$\bar{D}_5$
1	1	0	0	$\bar{D}_6$
1	1	1	0	$\bar{D}_7$

74LS150 [16:1 MUX]

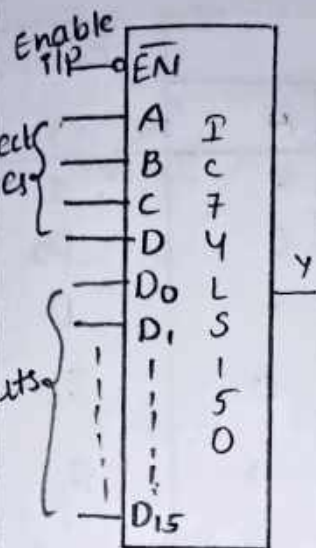
Block Diagram:-



Logic symbol:-

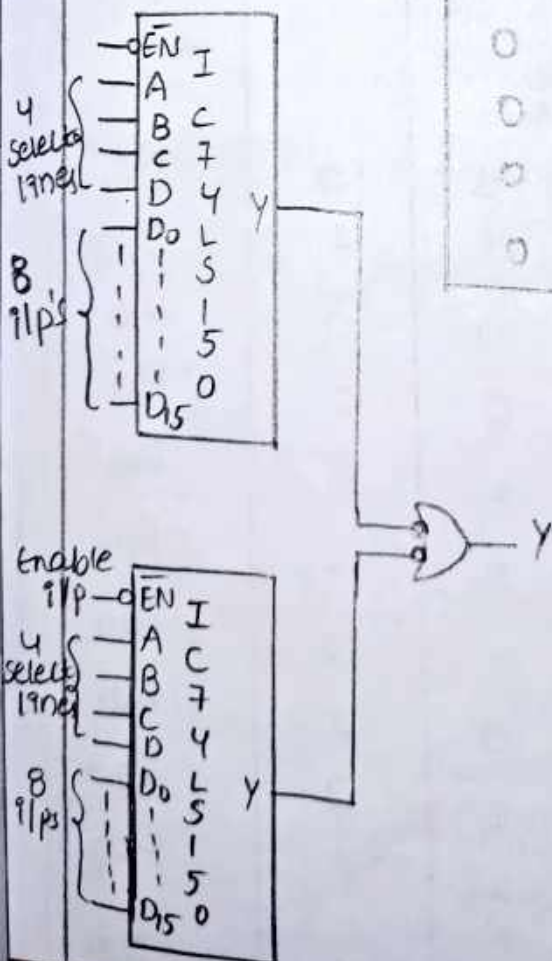
Truth Table:-

output



Inputs					output
$\bar{E}N$	D	C	B	A	Y
1	X	X	X	X	1
0	0	0	0	0	$\bar{D}_0$
0	0	0	0	1	$\bar{D}_1$
0	0	0	1	0	$\bar{D}_2$
0	0	0	1	1	$\bar{D}_3$
0	0	1	0	0	$\bar{D}_4$
0	0	1	0	1	$\bar{D}_5$
0	0	1	1	0	$\bar{D}_6$
0	0	1	1	1	$\bar{D}_7$
0	1	0	0	0	$\bar{D}_8$
0	1	0	0	1	$\bar{D}_9$
0	1	0	1	0	$\bar{D}_{10}$
0	1	0	1	1	$\bar{D}_{11}$
0	1	1	0	0	$\bar{D}_{12}$
0	1	1	0	1	$\bar{D}_{13}$
0	1	1	1	0	$\bar{D}_{14}$
0	1	1	1	1	$\bar{D}_{15}$

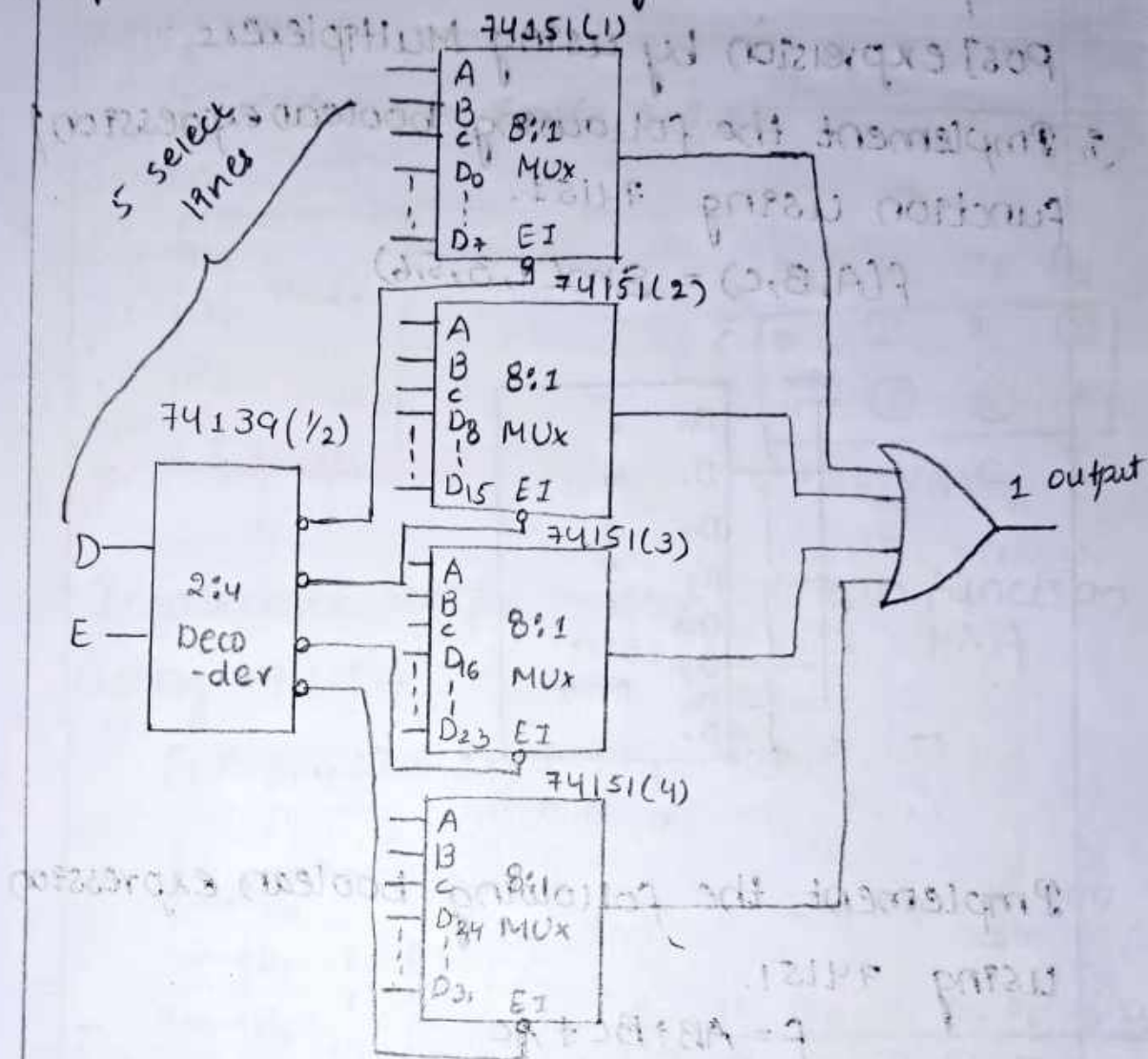
Implement 3a11
MUX using
IC 74LS150



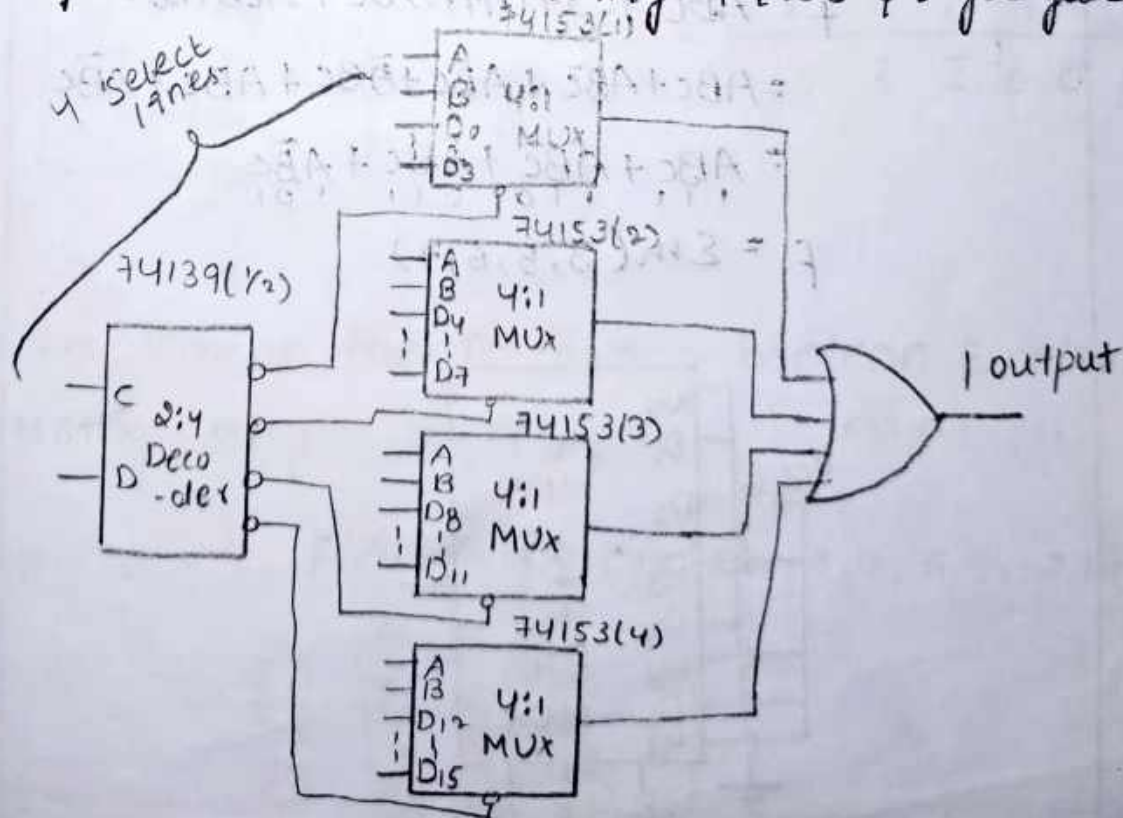
Truth Table:-

Inputs					Output
$\overline{EN}$	D	C	B	A	Y
X	X	X	X	X	1
0	0	0	0	0	D ₀
0	0	0	0	1	D ₁
0	0	0	1	0	D ₂
0	0	0	1	1	D ₃
0	0	1	0	0	D ₄
0	0	1	0	1	D ₅
0	0	1	1	0	D ₆
0	0	1	1	1	D ₇
0	1	0	0	0	D ₈
1					1
1					1
1					1
1	1	1	1	0	D ₁₄
0	1	1	1	1	D ₁₅
1	0	0	0	0	D ₁₆
1	0	0	0	1	D ₁₇
1	0	0	1	0	D ₁₈
1	0	0	1	1	D ₁₉
1	0	1	0	0	D ₂₀
1	0	1	0	1	D ₂₁
1	0	1	1	0	D ₂₂
1	0	1	1	1	D ₂₃
1	1	1	1	1	D ₃₁

Implement 32:1 MUX using 74151 and 74139



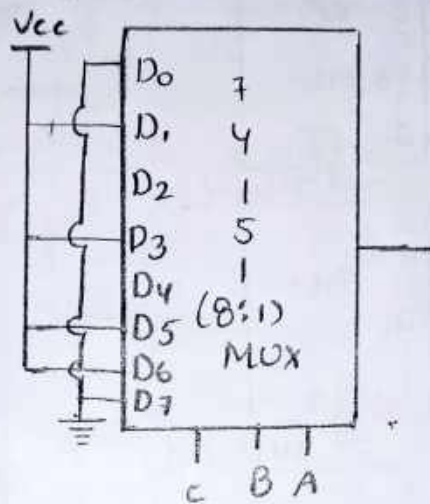
Implement 16:1 MUX using 74153 & logic gates



Implementation of Combinational [SOP, POS] expression by using Multiplexers

1. Implement the following boolean expression function using 74151.

$$f(A, B, C) = \sum m(1, 3, 5, 6)$$



Implement the following boolean expression using 74151.

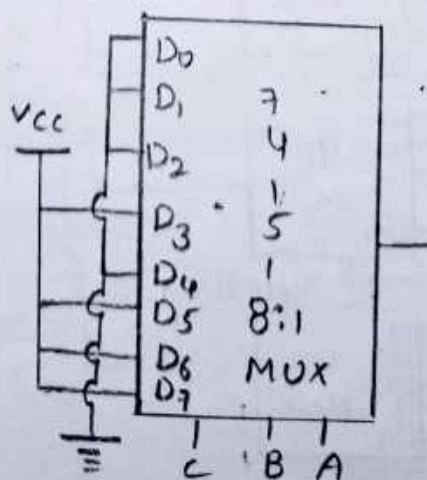
$$f = AB + BC + AC$$

$$f = AB(C + \bar{C}) + (A + \bar{A})BC + A(B + \bar{B})C$$

$$= ABC + AB\bar{C} + ABC + \bar{A}BC + ABC + A\bar{B}C$$

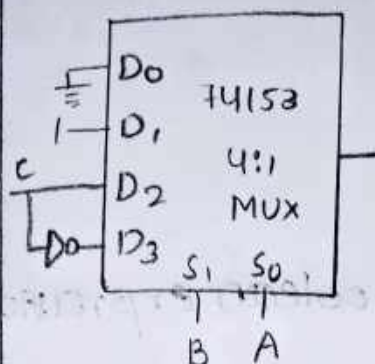
$$= ABC + AB\bar{C} + \bar{A}BC + A\bar{B}C$$

$$f = \sum m(3, 5, 6, 7)$$



Implement the following boolean function using 74153.

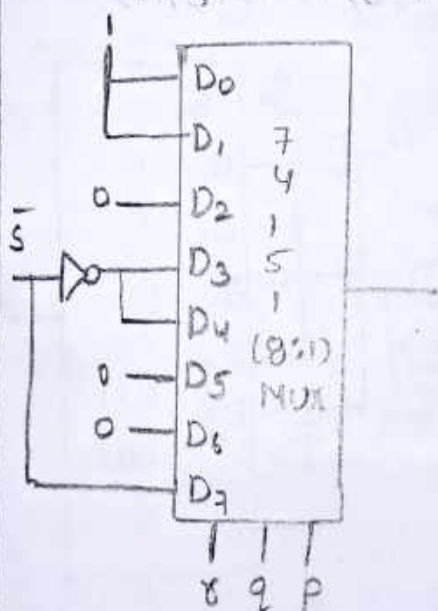
$$F(A, B, C) = \sum m(1, 3, 5, 6)$$



	D ₀	D ₁	D ₂	D ₃
$\bar{C}$	0	①	2	③
C	4	⑤	⑥	7

Implement the following boolean function using 74151.

$$F(P, Q, R, S) = \sum m(0, 1, 3, 4, 8, 9, 15)$$



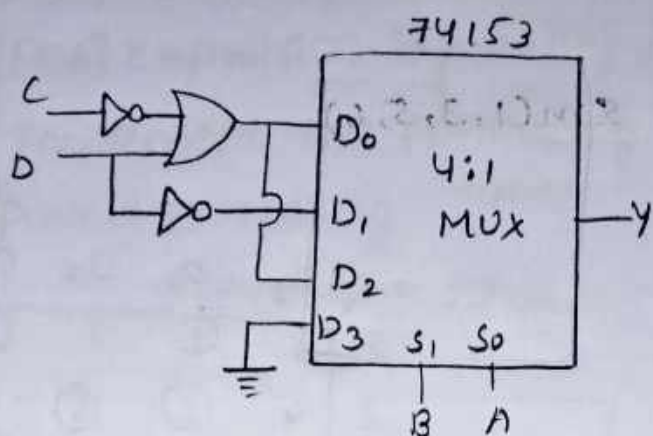
Implementation Table

	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
$\bar{S}$	①	②	2	③	④	5	6	7
S	⑧	⑨	10	11	12	13	14	⑮

Implement the following boolean function using single 74153.

$$F(A, B, C, D) = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$$

	D ₀	D ₁	D ₂	D ₃
$\bar{C}\bar{D}$	①	②	③	4
$\bar{C}D$	⑤	⑥	7	8
$C\bar{D}$	⑨	10	11	12
CD	13	⑭	15	16



Implement the following boolean expression using 74151.

$$F(A, B, C, D) = \pi M(0, 3, 5, 8, 9, 10, 12, 14)$$

↓ pos

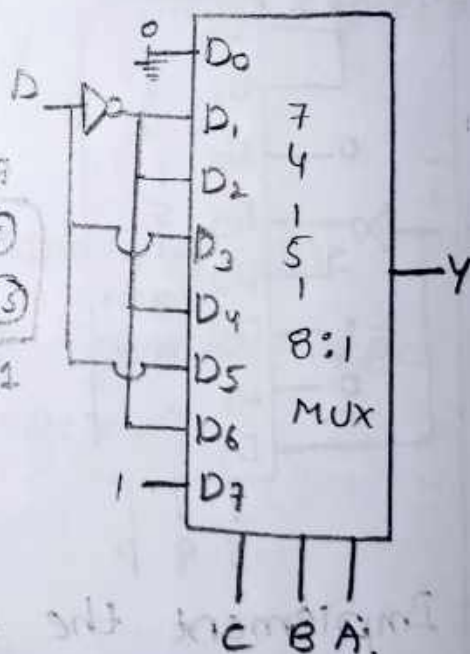
↓ Max terms

$$F(A, B, C, D) = \Sigma m(1, 2, 4, 6, 7, 11, 13, 15)$$

Implementation

Table

	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
$\bar{D}$	0	①	②	3	④	5	⑥	⑦
D	8	9	10	⑪	12	⑬	14	⑮
	0	$\bar{D}$	$\bar{D}$	D	$\bar{D}$	D	$\bar{D}$	1

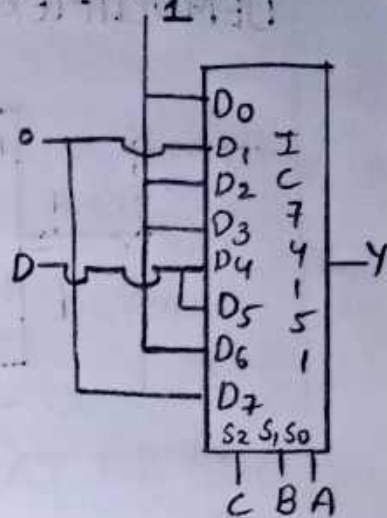


Implement the following Boolean function using 74151

$$F(A, B, C, D) = \Sigma m(0, 2, 6, 10, 11, 12, 13) + d(3, 8, 14)$$

Implementation Table

	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
$\bar{D}$	0	1	2	3	4	5	6	7
D	8	9	10	11	12	13	14	15
	1	0	1	1	0	0	1	0



Implement the following function using IC 74151 [8:1 MUX].

$$F(A, B, C, D) = \bar{A}\bar{B}\bar{D} + ACD + \bar{B}CD + \bar{A}\bar{C}D$$

$$F(A, B, C, D) = \bar{A}\bar{B}\bar{D} + ACD + \bar{B}CD + \bar{A}\bar{C}D$$

$$\Rightarrow \bar{A}B(C + \bar{C})\bar{D} + A(B + \bar{B})CD + (A + \bar{A})\bar{B}CD + \bar{A}(B + \bar{B})\bar{C}D$$

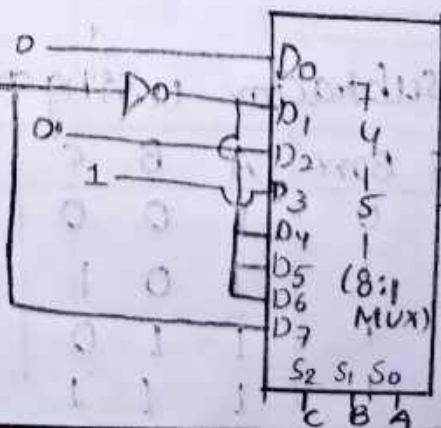
$$\Rightarrow \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + \bar{A}BCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D + AB\bar{C}\bar{D} + AB\bar{C}D$$

$$\Rightarrow \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + \bar{A}BCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D + AB\bar{C}\bar{D} + AB\bar{C}D$$

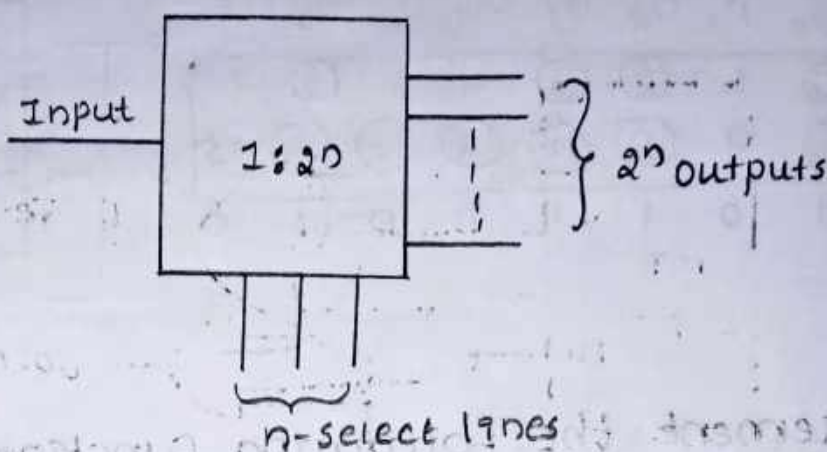
$$F(A, B, C, D) = \sum m(1, 3, 4, 5, 6, 11, 15)$$

Implementation Table:

	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
$\bar{D}$	0	1	2	3	4	5	6	7
D	8	9	10	11	12	13	14	15
	0	1	0	1	0	0	0	0



DEMULTIPLEXER:-



Types of DE-MUX:-

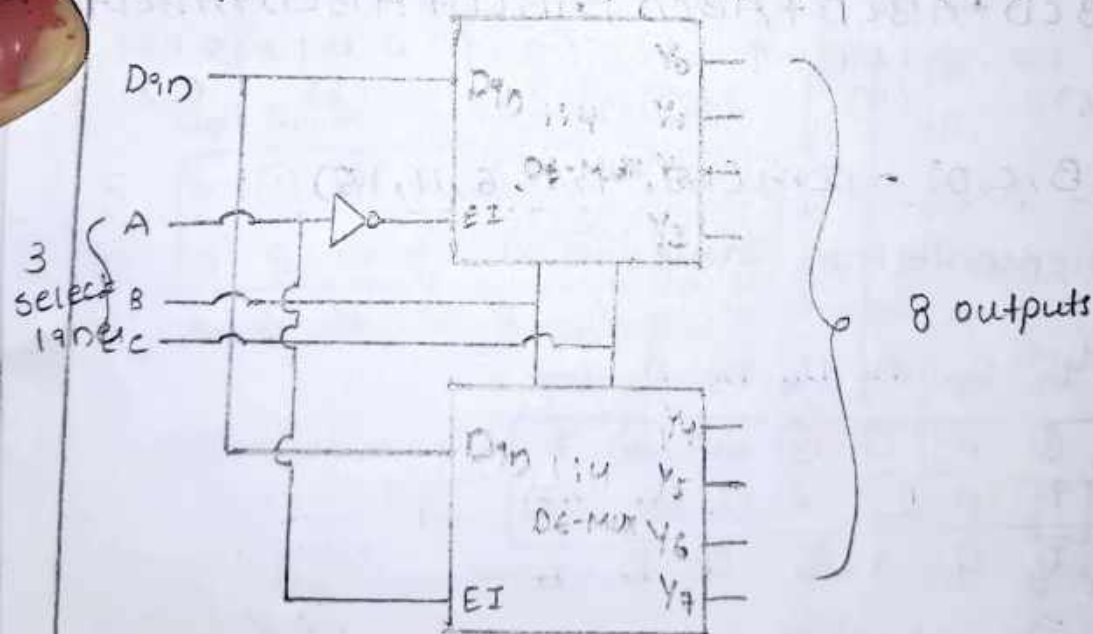
$1:2^n$

$n=1 \Rightarrow 1:2$

$n=2 \Rightarrow 1:4$

$n=3 \Rightarrow 1:8$

Implement $1:8$ DE-MUX using $1:4$ DE-MUX.

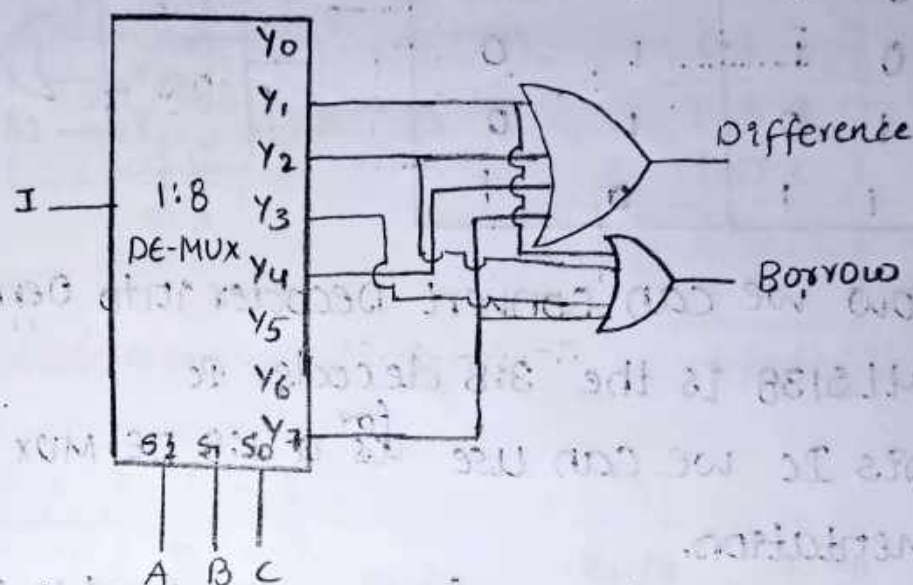


Implement full subtractor using DE-MUX

A	B	C	Diff	Borr	A	B	C	Diff	Borr
0	0	0	0	0	1	0	0	1	0
0	0	1	1	1	1	0	1	0	0
0	1	0	1	1	1	1	0	0	0
0	1	1	0	1	1	1	1	1	1

$$\text{Diff} = \sum m(1, 2, 4, 7)$$

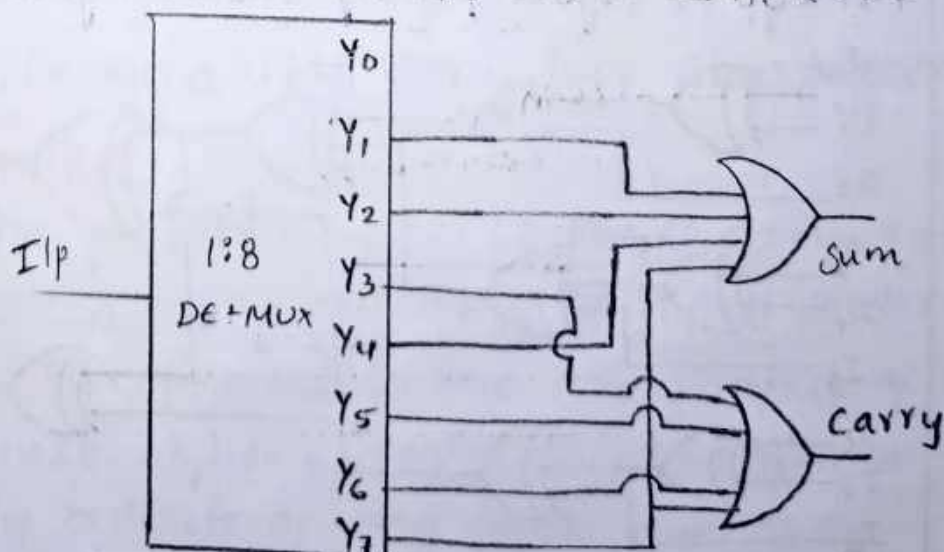
$$\text{Borrow} = \sum m(1, 2, 3, 7)$$



Implement the Full adder using DE-MUX

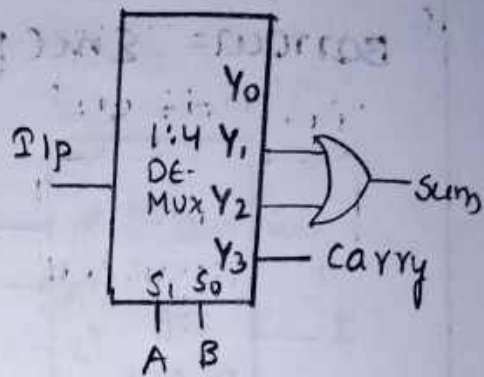
A	B	C	Sum	Carry	A	B	C	Sum	Carry
0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1
0	1	1	0	1	1	1	1	1	1

$$\text{Sum} = \sum m(1, 2, 4, 7) ; \text{Carry} = \sum m(3, 5, 6, 7)$$



Implement the Half-Adder using DE-MUX.

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



How we can convert Decoder into Demultiplexer

74LS138 is the 3:8 decoder IC

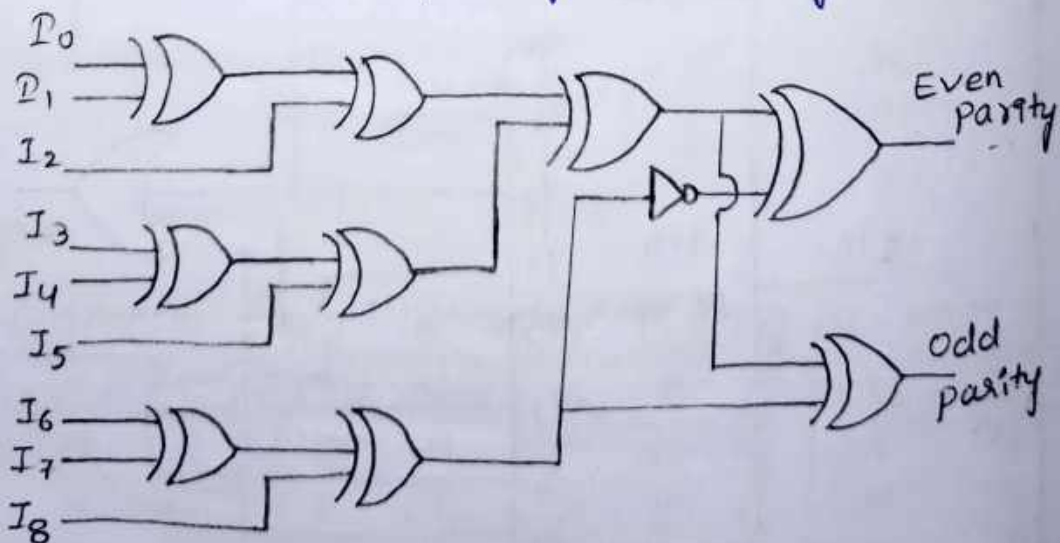
This IC we can use ^{for} as a 1:8 DE-MUX implementation.

In 3:8 decoder we have a one enable input, that can be considered as a single input of 1:8 DE-MUX and 3 inputs of 3:8 ^{decoder} can be used as 3 select lines of 1:8 DE-MUX.

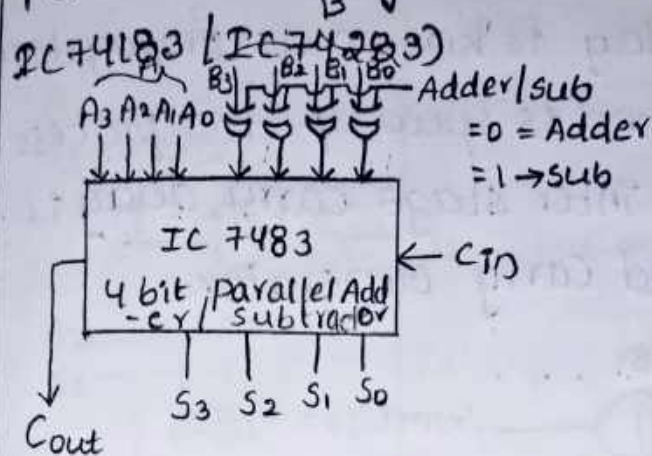
Outputs of 3:8 decoder & 1:8 Demultiplexer are same.

Parity Generator / Checker:-

74x280 → 9 bit parity checker / generator



Parallel Binary Adder / Subtractor :- (IC 7483)



Subtraction :-

$$\begin{array}{r}
 1110 \quad 14 \\
 0110 \quad 6 \\
 \hline
 1000 \quad 8 \\
 1001 \\
 \hline
 1 \quad 0111 \\
 \hline
 1000 \quad +8
 \end{array}$$

Addition :-

$$\begin{array}{r}
 1011 \quad 11 \\
 0111 \quad 7 \\
 \hline
 10010 \quad 18
 \end{array}$$

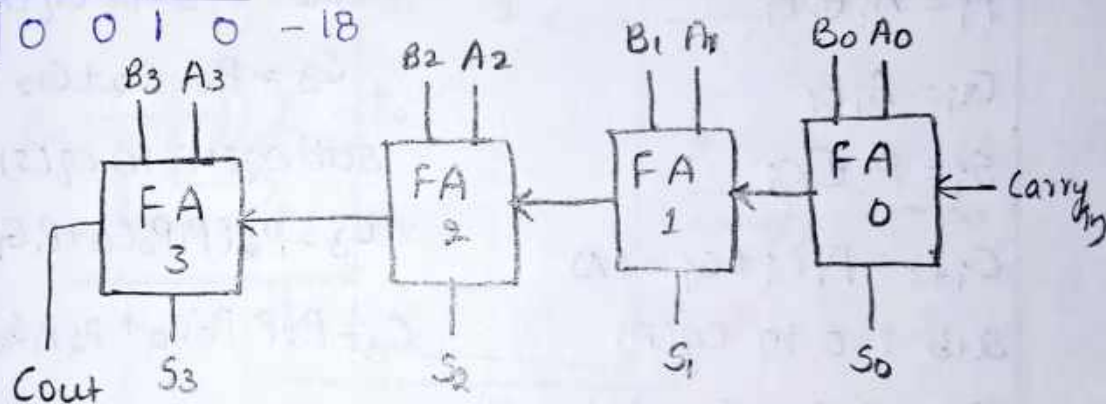


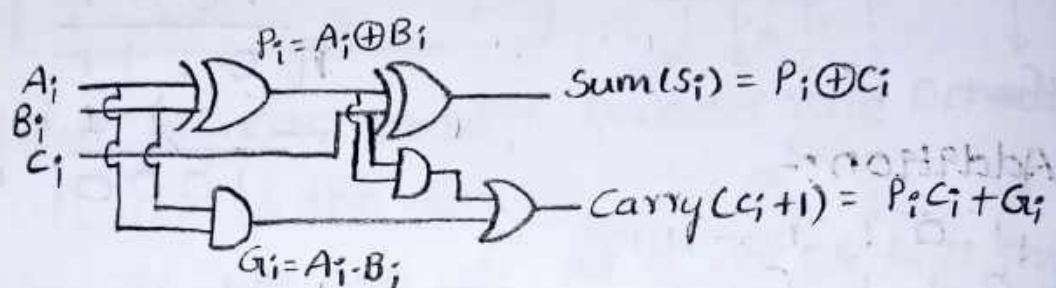
Fig:- Internal structure

Parallel Adder → Ripple Carry Adder

What do you mean by carry propagation delay. Design a 4 bit carry look ahead generator [IC 74182].

The parallel adder is ripple carry type in which carry output of each full adder is connected to the carry input of the next higher order stage. The sum and carry outputs of any stage cannot be produced until the input carry occurs.

This leads to a time delay in addition process. This delay is known as propagation delay. One method is speed up this process by eliminating inter stage carry delay is called look ahead Carry Generator.



$$P_i = A_i \oplus B_i$$

$$G_i = A_i \cdot B_i$$

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = P_i C_i + G_i \quad \text{--- (A)}$$

sub $i=0$ in eq(A)

$$C_1 = P_0 C_0 + G_0 \quad \text{--- (2)}$$

Sub $i=1$ in eq(A)

$$C_2 = P_1 C_1 + G_1 \quad \text{--- (3)}$$

Sub eq(3) in eq(2)

$$C_2 = P_1 (P_0 C_0 + G_0) + G_1$$

$$= P_1 P_0 C_0 + P_1 G_0 + G_1 \quad \text{--- (4)}$$

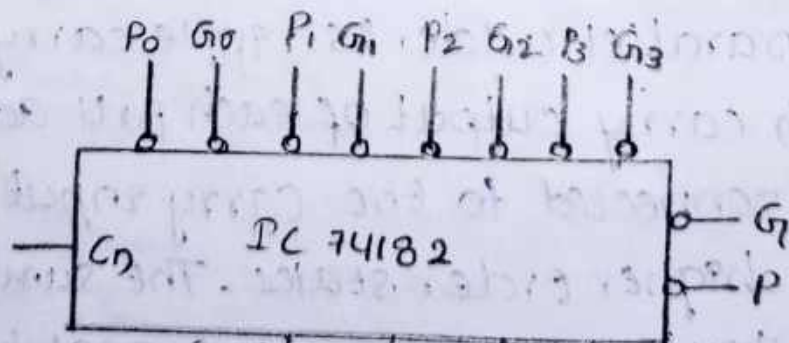
Sub $i=2$ in eq(A)

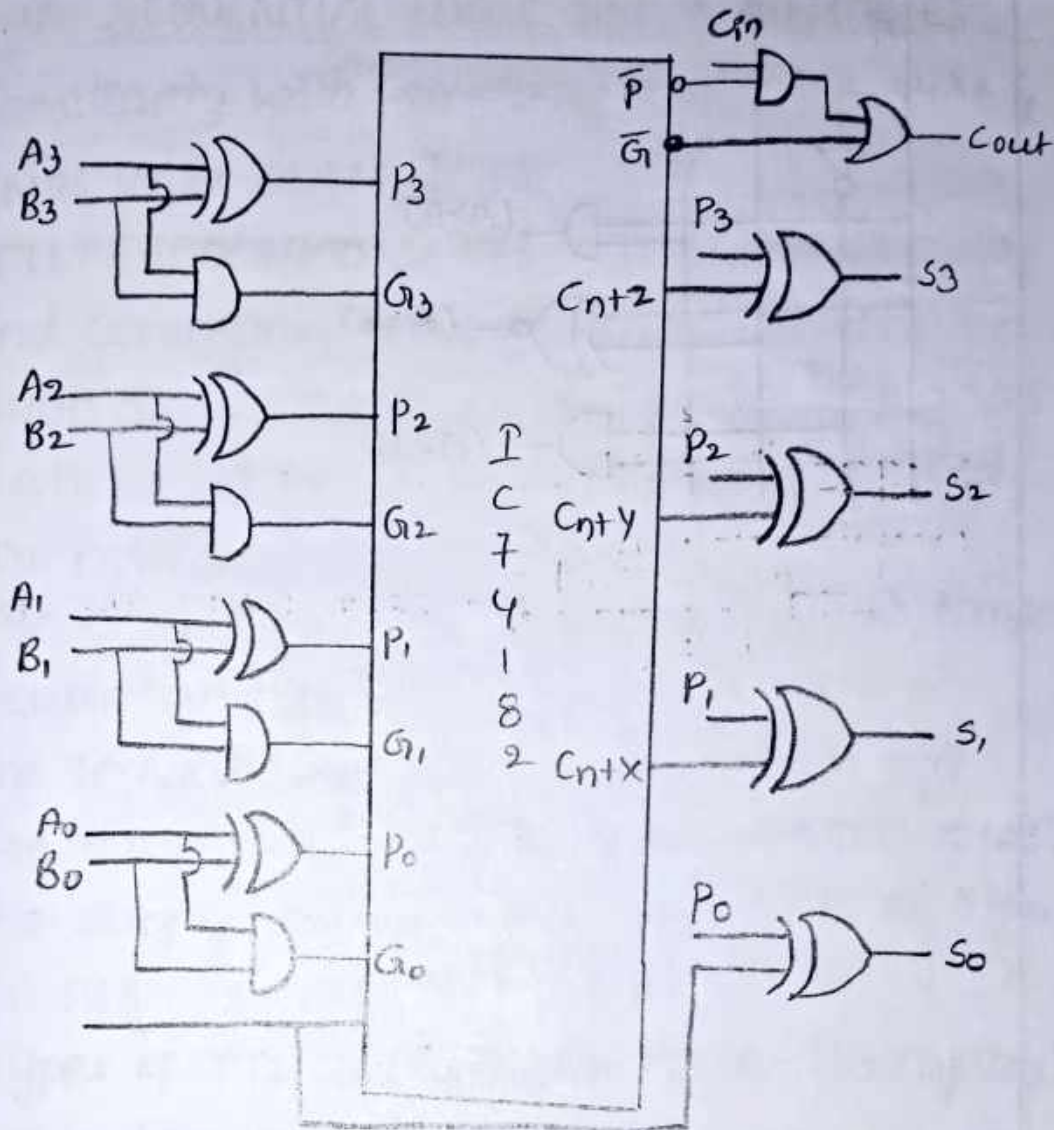
$$C_3 = P_2 C_2 + G_2 \quad \text{--- (5)}$$

sub eq(4) in eq(5)

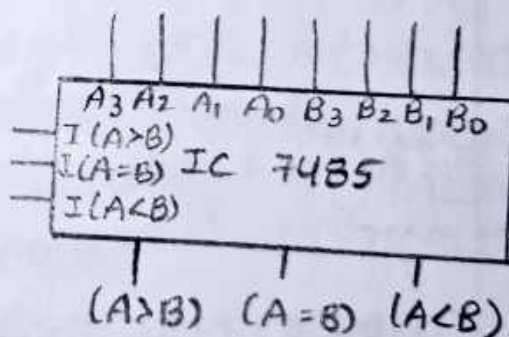
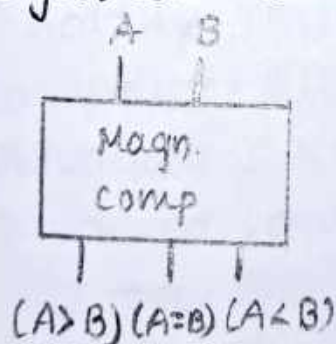
$$C_3 = P_2 (P_1 P_0 C_0 + P_1 G_0 + G_1) + G_2$$

$$C_3 = P_2 P_1 P_0 C_0 + P_2 P_1 G_0 + P_2 G_1 + G_2$$





Magnitude Comparator:-



Design of 1 bit Comparator.

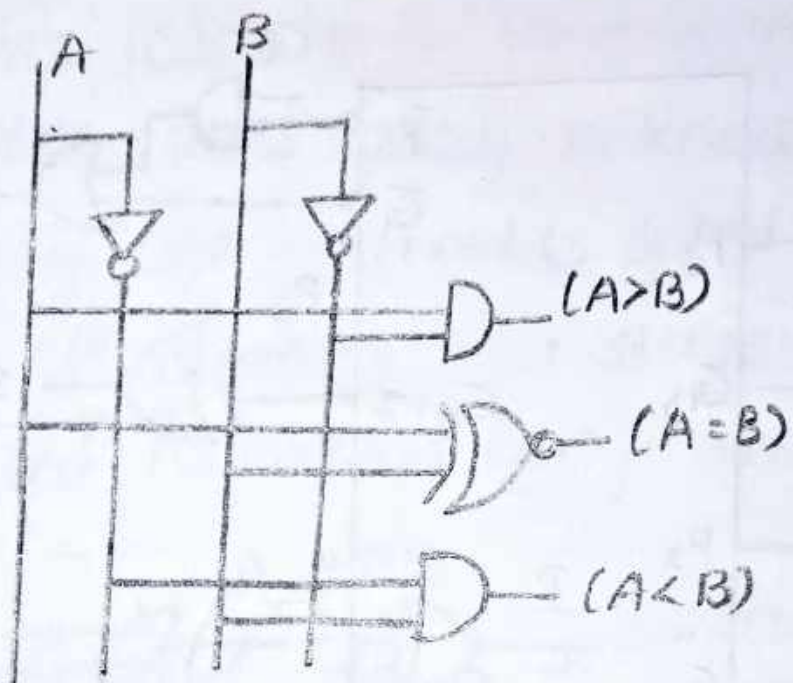
Inputs		Outputs		
A	B	(A > B)	(A = B)	(A < B)
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

$$A > B = \overline{A}B$$

$$A = B = \overline{A}\overline{B} + AB$$

$$= A \odot B$$

$$A < B = A\overline{B}$$



V. SEQUENTIAL LOGIC IC'S & MEMORIES

Familiarity with commonly available 74xx & CMOS 40xx series ICs:-

TTL 5400/7400 series is the most popular and commonly used series of digital IC. 7400 devices are used for commercial applications whereas 54xx devices are used for military applications.

The only difference in this series are temperature and power supply ranges.

The temperature for 7400 is 0°C to 70°C

The temperature for 5400 is -55°C to $+125^{\circ}\text{C}$.

The supply voltage range for 74xx is $5 \pm 0.25\text{V}$ for 54xx $5 \pm 0.5\text{V}$

Types of TTL ICs (Bipolar logic family ICs):-

1. Standard TTL (5400/7400)
2. Schottky TTL (54S00/74S00)
3. Low power (LT) Schottky TTL (54LS00/74LS00)
4. Advanced Schottky TTL (54AS00/74AS00)
5. Advanced Low Power Schottky TTL (54ALS00/74ALS00)
6. Fast TTL (54F00/74F00)

Characteristics of TTL families (Bipolar)

Parameter	7400	74S00	74LS00	74AS00	74ALS00	74F00
Propagation delay (nsec)	9	3.8	9.5	1.7	1.4	3
Power dissipation (mW)	10	20	2	8	2	6

Parameter	7400	74LS	74ALS	74AS	74ALS	74F
Speed-power product (PT)	90	60	19	13.6	4.8	18
Maximum clock rate (MHz)	35	125	45	200	70	100
Fan out	10	10/20	20	40	20	33
voltage parameters						
$V_{OH}(min) - V$	2.4	2.7	2.7	2.5	2.5	2.5
$V_{OL}(max) - V$	0.4	0.4	0.5	0.5	0.4	0.5
$V_{IH}(min) - V$	2	2	2	2	2	2
$V_{IL}(max) - V$	0.8	0.8	0.8	0.8	0.8	0.8

CMOS Series (4000/14000)

4000B - Basic CMOS Series

74CMOS Series - (Standard)

74HC/HCT → High speed CMOS / High speed CMOS with TTL compatibility

74AC/ACT → Advanced CMOS / Advanced CMOS with TTL compatibility

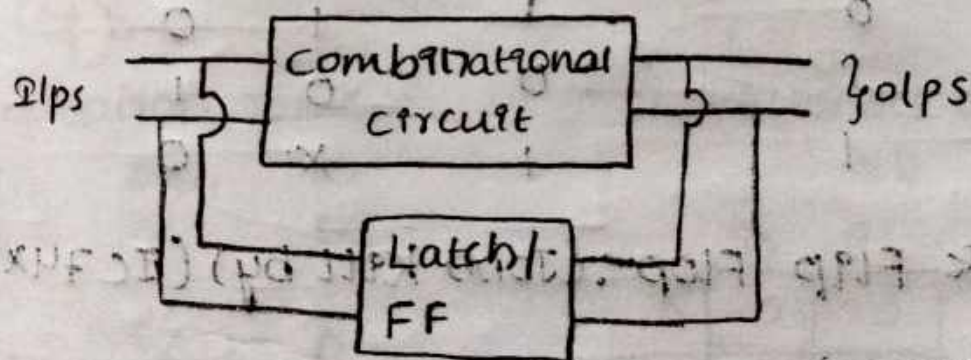
Characteristics of CMOS families (unipolar)

Parameter	4000B	74HC	74HCT	74AC	74ACT
propagation delay (nsec)	50	8	8	4.7	4.7
power dissipation (mw)	0.1	0.17	0.17	0.08	0.08
Speed-power product (PT)	5	1.36	1.36	0.376	0.376

Parameter	400BB	74HC	74HCT	74AC	74ACT
Maximum clock rate (MHz)	12	40	40	100	100
Voltage	0	0	0	1	
Parameters - (V)	1	1	0	1	
V_{OH} (mA)	4.9	4.9	4.9	4.9	4.9
V_{OL} (max)	0.05	0.1	0.1	0.1	0.1
V_{IH} (mA)	3.5	3.5	2	3.5	2
V_{IL} (max)	1.5	1	0.8	1.5	0.8

Sequential circuit

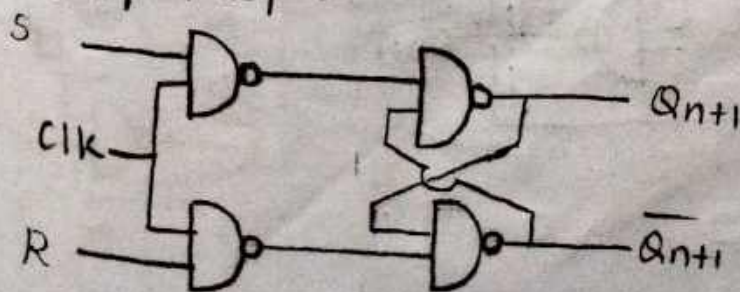
Any digital circuit output depends upon the present input as well as past inputs & output variables that is called sequential circuit. To remember the previous information there is a memory elements (latch / Flip Flop).



Block diagram of sequential circuit

Flip Flops :-

SR Flip Flop :-



Logic diagram



Truth Table

Clk	S	R	Q_n	Q_{n+1}
↑	0	0	0	0
↑	0	0	1	1
↑	0	1	0	0
↑	0	1	1	0
↑	1	0	0	1
↑	1	0	1	1
↑	1	1	0	X
↑	1	1	1	X

	$\bar{R}\bar{A}_n$	$\bar{R}A_n$	$R\bar{A}_n$	RA_n
$\bar{S}$	0	1	0	0
S	1	1	X	X

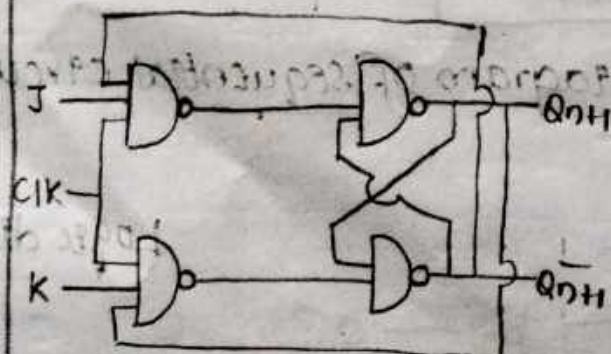
Characteristic equation = $S + \bar{R}Q_n$

Inambiguous state

Excitation Table of SR Flip Flop:-

Present State	Next State	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

JK Flip Flop: (John Kill by) (IC 74x73)



Truth Table

Inputs				Output
clk	J	K	Q_n	Q_{n+1}
↑	0	0	0	0
↑	0	0	1	1
↑	0	1	0	0
↑	0	1	1	0
↑	1	0	0	1
↑	1	0	1	1
↑	1	1	0	1
↑	1	1	1	0

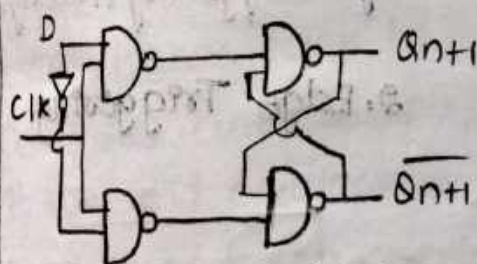
	$\bar{K} \bar{Q}_n$	$\bar{K} Q_n$	$K \bar{Q}_n$	$K Q_n$
$\bar{J}$	0	1	0	0
J	1	1	0	1

characteristic equation = $J \bar{Q}_n + \bar{K} Q_n$

Excitation Table

P_s	M_s	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D Flip Flop (IC 74874)



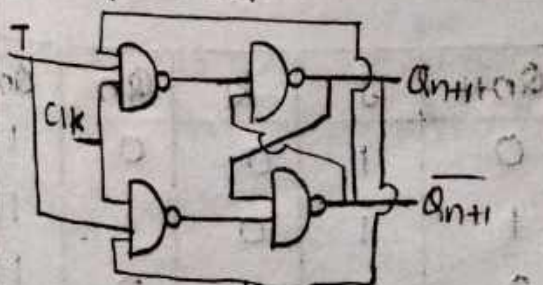
Excitation Table :-

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

characteristic eqn = D

	$\bar{Q}_n$	Q_n
$\bar{D}$	0	0
D	1	1

T Flip Flop



Truth Table

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table

	$\bar{Q}_n$	Q_n
$\bar{T}$	0	1
T	1	0

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

$$Q_{n+1} = \bar{T}Q_n + T\bar{Q}_n$$

$$\text{change} = T \oplus Q_n$$

Clock, Triggering

Trigger is used to activate the flipflop.

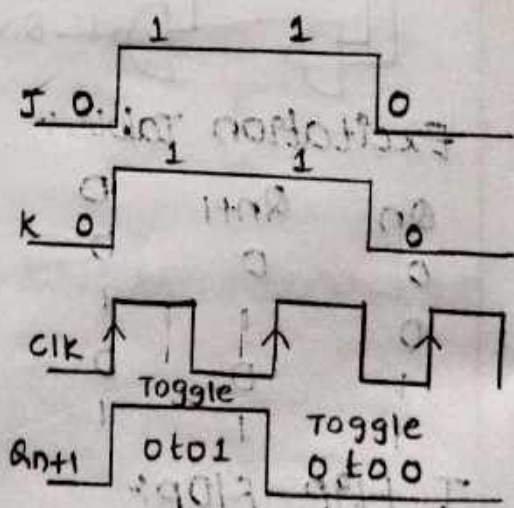
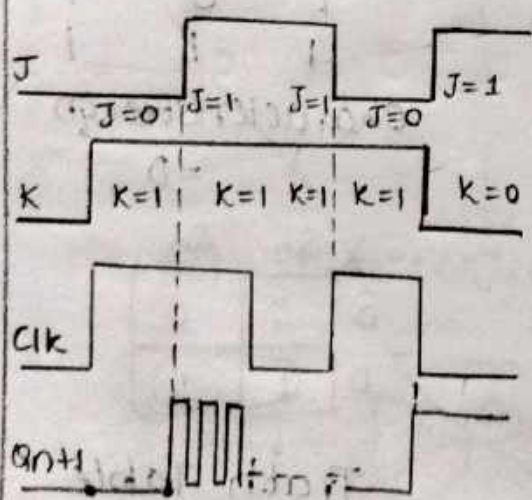
There are two types of triggering methods.

1. Level Triggering
 Positive level triggering
 Negative level triggering

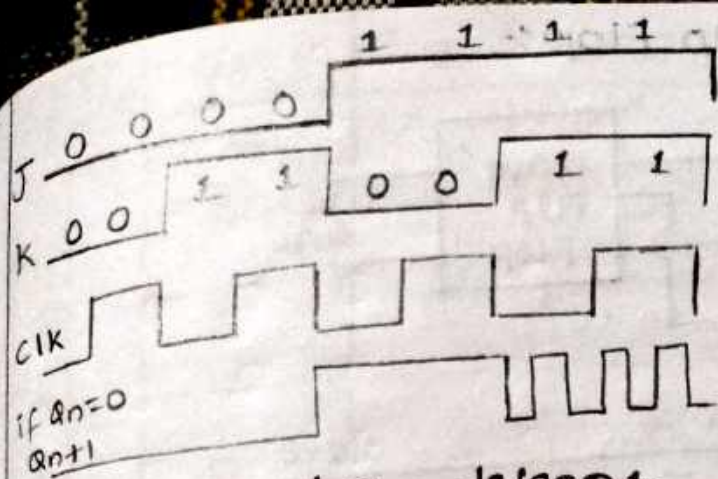
2. Edge Triggering
 +ve edge triggering [Rising edge]
 -ve edge triggering [falling edge]

1. Level Triggering

2. Edge Triggering



J	K	Q_n	Q_{n+1}	J	K	Q_n	Q_{n+1}
0	0	0	0	1	0	0	1
0	0	1	1	1	0	1	1
0	1	0	0	1	1	0	1
0	1	1	0	1	1	1	0



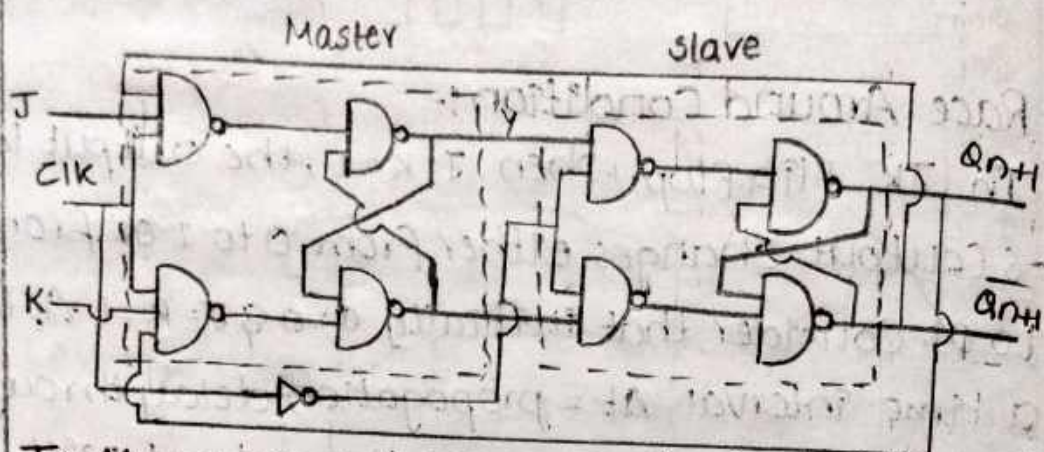
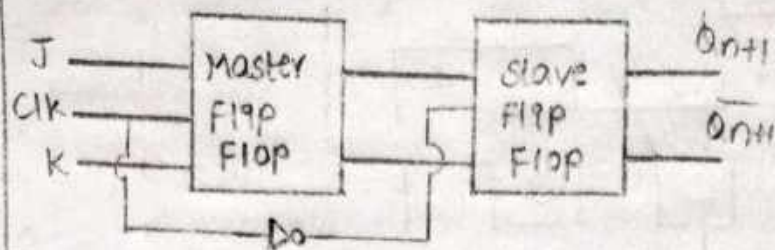
Race Around Condition:-

In JK Flip Flop, when $J=K=1$, the output toggles (output changes either from 0 to 1 or from 1 to 0). Consider that initially $Q=0$ & $J=K=1$. After a time interval $\Delta t = \text{propagation delay through two NAND gates in series}$ the output will change to $Q=1$. And, after another time interval of Δt the output will change back to $Q=0$. This toggling will continue until the flip flop is disabled & $J=K=1$. At the end of clock of the Flip Flop is disabled & value of Q is uncertain (we can't predict that the output is 0 or 1). This situation is referred to as race around condition.

This condition exists, when $t_p \geq \Delta t$. Thus by keeping $t_p < \Delta t$ we can avoid race around condition.

We can keep $t_p < \Delta t$ by keeping the duration of edge less than Δt . A more practical method to overcome this difficulty is use of master slave configuration.

Master-slave Flip Flop:-

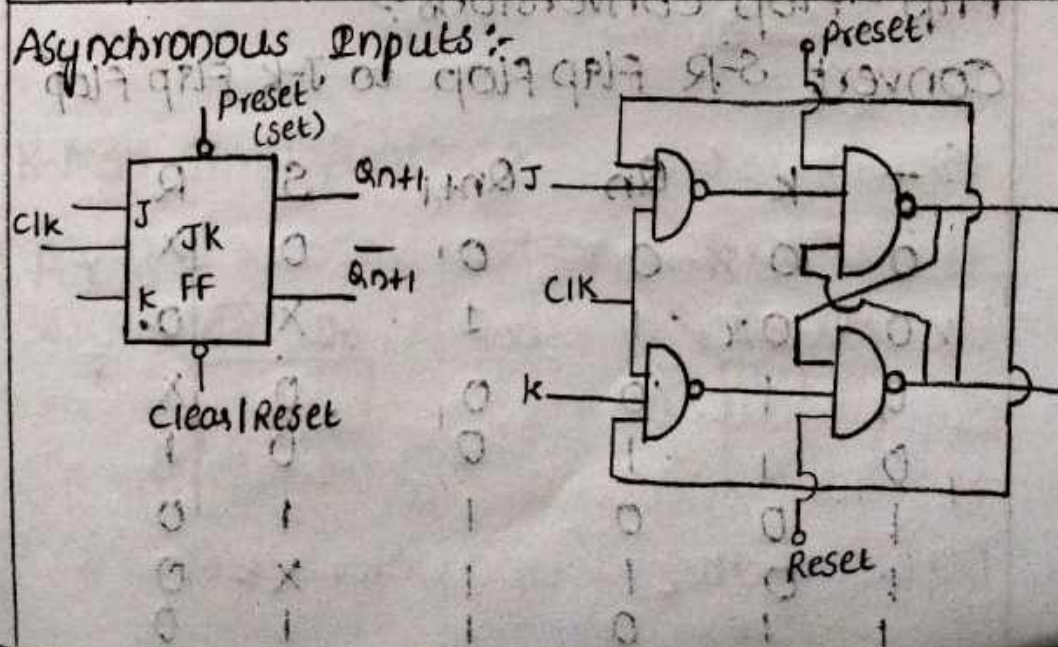


Truth Table for Master slave JK Flip Flop

Clock pulse	Q_n	J	K	Master output Q	Slave output Q_{n+1}
	0	0	0	0	NC
	0	0	0	NC	0
	1	0	0	1	NC
	1	0	0	NC	1
	0	0	1	0	NC
	0	0	1	NC	0

Clock Pulse	Qn	J	K	Master o/p Y	Slave o/p Qn+1
	1	0	1	0	NC
	1	0	1	NC	0
	0	1	0	1	NC
	0	1	0	NC	1
	1	1	0	1	NC
	1	1	0	NC	1
	0	1	1	1	NC
	0	1	1	NC	1
	1	1	1	0	NC
	1	1	1	NC	0

Asynchronous Inputs:-



For all the Flip Flops [SR, JK, T, D] all the inputs are called synchronous ips. Because data on these inputs are transferred to the flip flop output only on the triggering edge of the clock pulse, i.e., the data are transferred synchronously with the clock.

Flip Flop available in IC packages sometimes provide special inputs for setting [Preset] or clearing [Clear ip] the flip flop asynchronous input. These inputs are called asynchronous or direct inputs. These inputs are connected directly into the latch portion of the flip flop so that they override the effect of synchronous inputs J, K & clock.

If preset & clear inputs are 1 the clock circuit operates in accordance with the truth table of JK Flip Flop [Normal JK FF operation].

If $\overline{\text{preset}} = 0$ & $\overline{\text{clear}} = 1$ the output of NAND gate '3', will set the output as 1. In this way we are setting the flip flop output Q_{n+1} by giving $\overline{\text{preset}}$ as 0.

Flip - Flop Conversions :-

Convert S-R Flip Flop to J-K Flip Flop

J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0

J	K	Qn	Qn+1	S	R
1	1	1	0	0	1

K-map simplification

For S:-

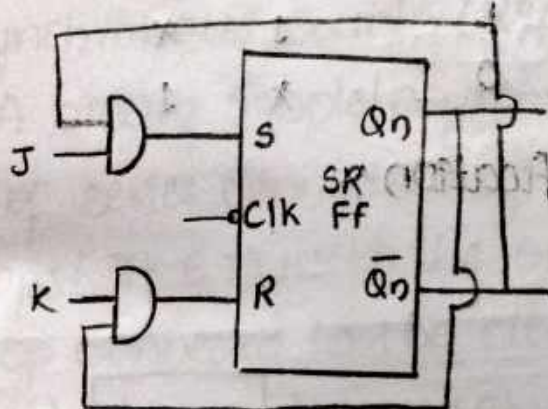
	$\bar{K}Q_n$	$K\bar{Q}_n$	KQ_n	$\bar{K}\bar{Q}_n$
$\bar{J}$	0	x	0	0
J	1	x	0	1

$$S = J\bar{Q}_n$$

For R:-

	$\bar{K}Q_n$	$K\bar{Q}_n$	KQ_n	$\bar{K}\bar{Q}_n$
$\bar{J}$	x	0	1	x
J	0	0	1	0

$$R = KQ_n$$



Conversion of SR Flip Flop to D Flip Flop

D	Qn	Qn+1	S	R
0	0	0	0	x
0	1	0	0	1
1	0	1	1	x
1	1	1	x	0

$\bar{D}$	Q_n	Q_{n+1}
1	0	1
0	1	0

K-Map simplification:-

For S:-

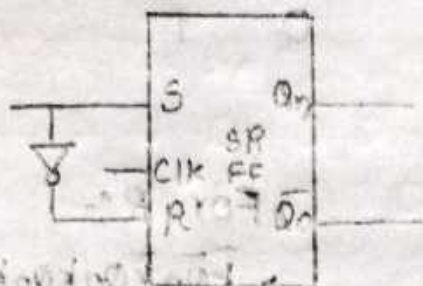
	$\bar{Q}_n$	Q_n
$\bar{D}$	0	0
D	1	x

$$S = D$$

For R:-

	$\bar{Q}_n$	Q_n
$\bar{D}$	x	1
D	0	0

$$R = \bar{D}$$



Convert JK Flip Flop to T Flip Flop

T	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

k-map Simplification:-

For J:-

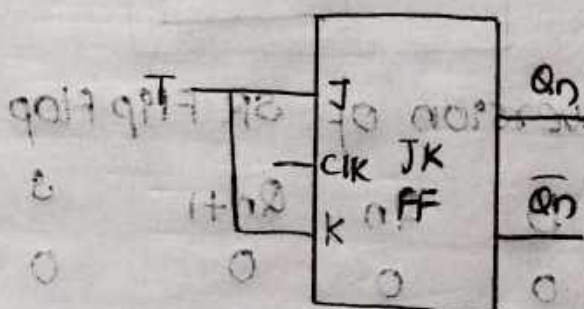
	$\bar{Q}_n$	Q_n
$\bar{T}$	0	X
T	1	X

$$J = T$$

For K:-

	$\bar{Q}_n$	Q_n
$\bar{T}$	X	0
T	X	1

$$K = T$$



Counters:-

A counter is a register capable of counting the number of clock pulses arriving at its clock input. Counter represents the number of clock pulses arrived. On arrival of each pulse in case of upcounter, the counter is

incremented by 1 and in case of down counter the counter is decremented by 1.

Types of counter:-

Counters

Asynchronous counter
(Ripple counter)

* JK & T Flip Flops
are used

Synchronous counter
(Parallel counter)

* All the Flip Flops
are used.

Asynchronous counter (Ripple Counter):-

A binary ripple/asynchronous counter consists of series connection of complementing flip-flops (JK & T) with the output of each flip-flop connected to the clock input of the next higher order flip-flop. The Flip Flop holding LSB [Least Significant Bit] receives the incoming clock pulses. A complementing Flip Flop can be obtained from JK Flip Flop with J and K tied together $J=K=1$ (or) from T Flip Flop $T=1$.

Design 3-bit asynchronous Up counter.

Step-1:- Logic diagram.

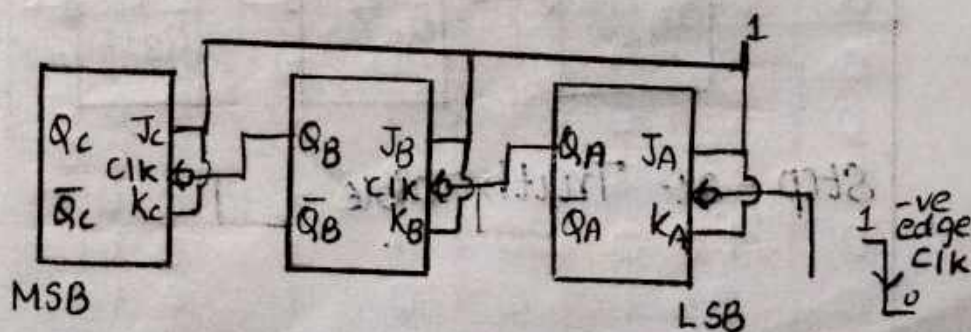
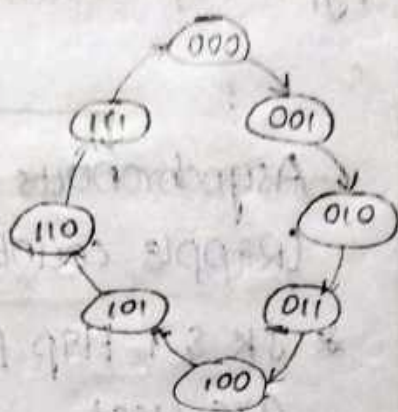


Fig: Logic Diagram 3-bit Asynchronous Up counter

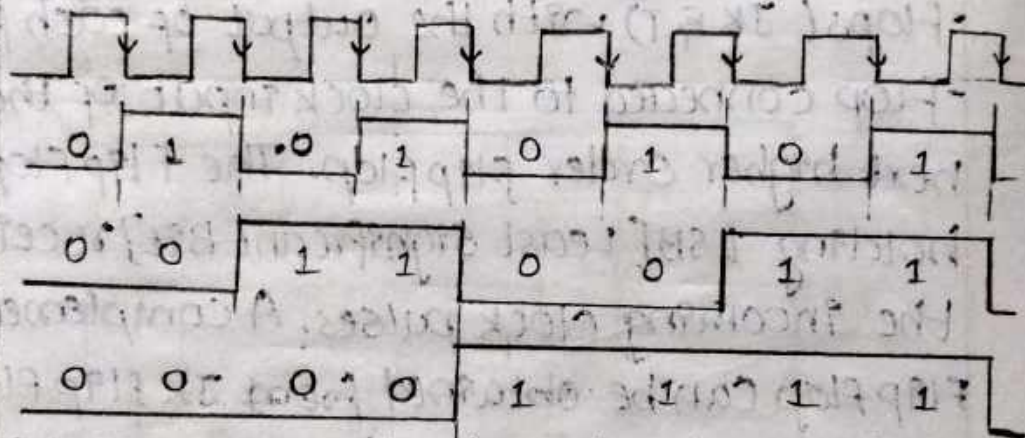
Step-2:- Truth Table

State diagram:-

CLK	PS Q _C	Q _B	Q _A	NS Q _{C+1}	Q _{B+1}	Q _{A+1}
0	0	0	0	0	0	1
1	0	0	1	0	1	0
2	0	1	0	0	1	1
3	0	1	1	1	0	0
4	1	0	0	1	0	1
5	1	0	1	1	1	0
6	1	1	0	1	1	1
7	1	1	1	0	0	0

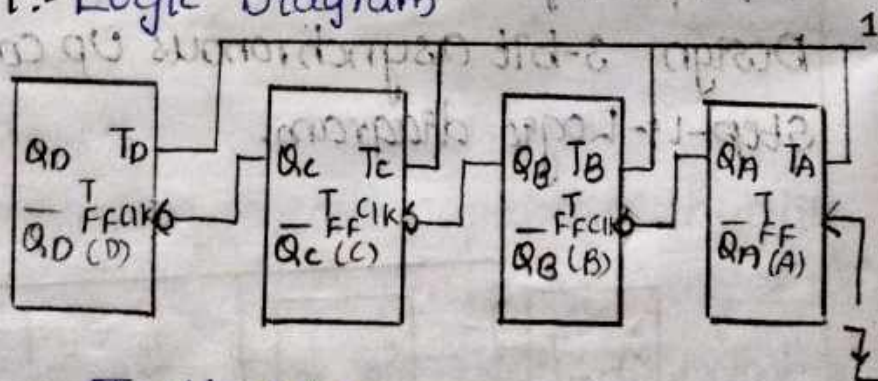


Timing diagram:-



Design a 4-bit Asynchronous down counter

Step-1:- Logic Diagram

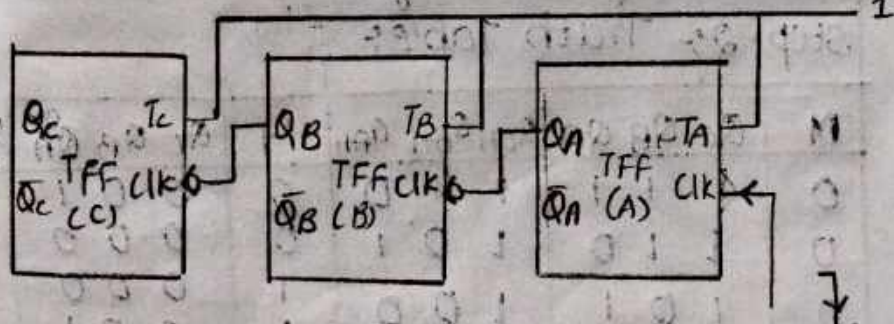


Step - 2:- Truth Table

clock	Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}
0	1	1	1	1	1	1	1	0
1	1	1	1	0	1	1	0	1
2	1	1	0	1	1	1	0	0
3	1	1	0	0	1	0	1	1
4	1	0	1	1	1	0	1	0
5	1	0	1	0	1	0	0	1
6	1	0	0	1	1	0	0	0
7	1	0	0	0	0	1	1	1
8	0	1	1	1	0	1	1	0
9	0	1	1	0	0	1	0	1
10	0	1	0	1	0	1	0	0
11	0	1	0	0	0	1	1	0
12	0	1	1	0	0	0	1	0
13	0	0	1	0	0	0	0	1
14	0	0	0	1	0	0	0	0
15	0	0	0	0	1	1	1	1

Design a 3-bit Asynchronous down counter by using negative edge clock pulse.

Step-1:- Logic Diagram

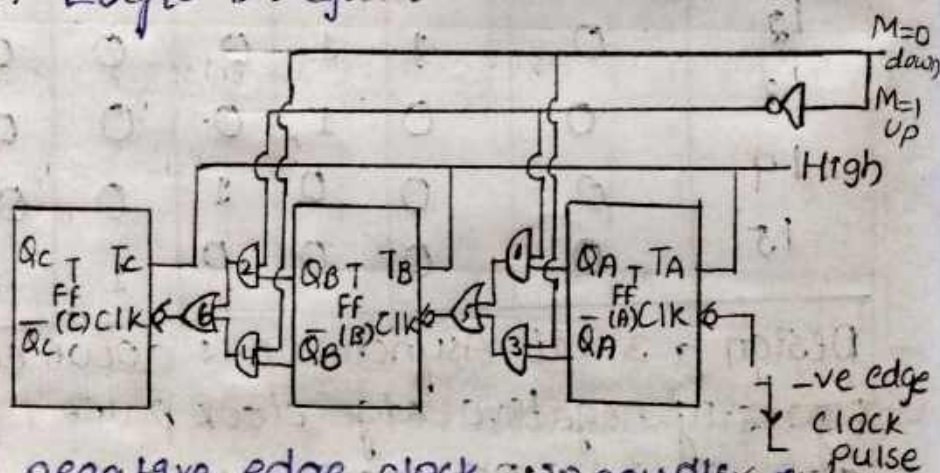


Step-2:- Truth Table

Clock	Q_C	Q_B	Q_A	Q_{CH}	Q_{BH}	Q_{AH}
0	1	1	1	1	1	0
1	1	1	0	1	0	1
2	1	0	1	1	0	0
3	1	0	0	0	1	1
4	0	1	1	0	1	0
5	0	1	0	0	0	1
6	0	0	1	0	0	0
7	0	0	0	1	1	1

Design 3-bit Asynchronous Up/down counter.

Step-1:- Logic Diagram



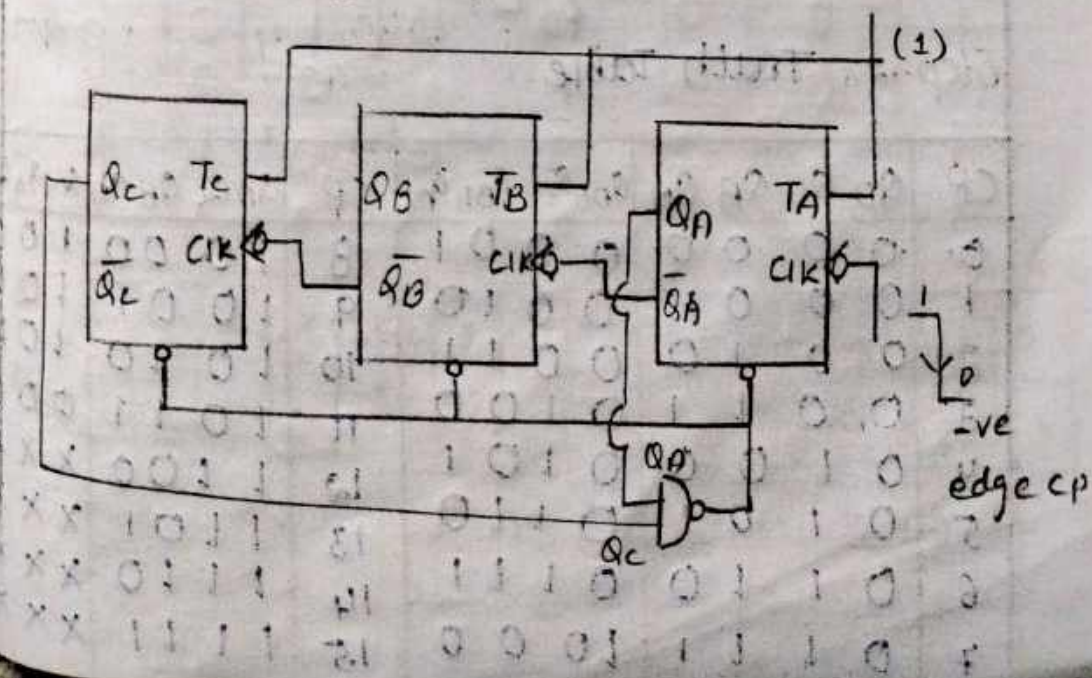
* For negative edge clock up counter Q_A .
for negative edge clock down counter $\bar{Q}_A$.

Step-2:- Truth Table:-

M	Q_C	Q_B	Q_A	Q_{CH}	Q_{BH}	Q_{AH}	M	Q_C	Q_B	Q_A	Q_{CH}	Q_{BH}	Q_{AH}
0	1	1	1	1	1	0	0	0	0	1	0	0	0
0	1	1	0	1	0	1	0	0	0	0	1	1	1
0	1	0	1	1	0	0	1	0	0	0	0	0	1
0	1	0	0	0	1	1	1	0	0	1	0	1	1
0	0	1	1	0	1	0	1	0	1	1	1	0	0
0	0	1	0	0	0	1	1	0	1	0	1	0	1
0	0	0	1	0	0	0	1	1	0	1	1	1	0
0	0	0	0	1	1	1	1	1	0	1	1	1	0

CP	Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	1	0	0
4	0	1	0	0	0	1	0	1
5	0	1	0	1	0	1	1	0
6	0	1	1	0	0	1	1	1
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	0	0	0	0
10	1	0	1	0	X	X	X	X
11	1	0	1	1	X	X	X	X
12	1	1	0	0	X	X	X	X
13	1	1	0	1	X	X	X	X
14	1	1	1	0	X	X	X	X
15	1	1	1	1	X	X	X	X

Design MOD-5 Asynchronous Down counter using T-Flip Flop



Step-2:- Truth Table

CP	PS			NS		
	Q _C	Q _B	Q _A	Q _{C+1}	Q _{B+1}	Q _{A+1}
0	1	0	0	0	1	1
1	0	1	1	0	1	0
2	0	1	0	0	0	1
3	0	0	1	0	0	0
4	0	0	0	1	0	0

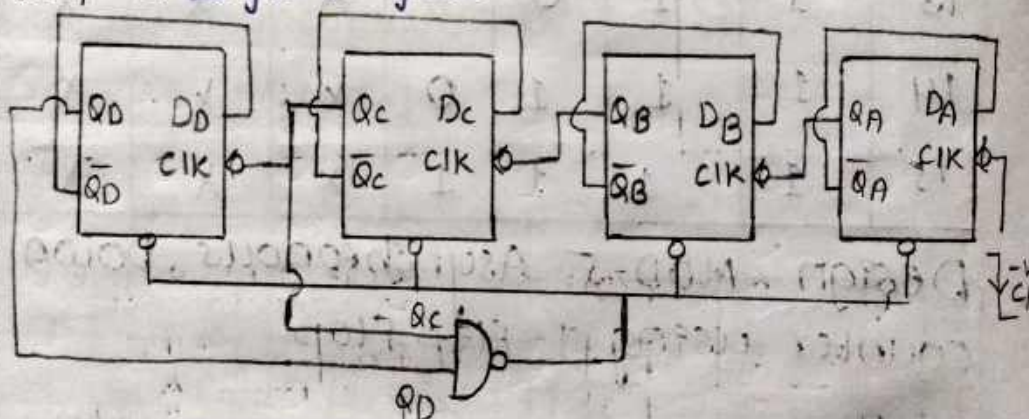
* 4 bit Ripple counter $\rightarrow$ IC 7493

IC 7493

* 4 bit Decade counter $\rightarrow$ IC 7490

Design MOD-12 ripple counter using IC 74x74.

Step-1:- Logic Diagram



Step-2:- Truth Table

CP	Q _D	Q _C	Q _B	Q _A	Q _{D+1}	Q _{C+1}	Q _{B+1}	Q _{A+1}	CP	Q _D	Q _C	Q _B	Q _A	Q _{D+1}	Q _{C+1}	Q _{B+1}	Q _{A+1}
0	0	0	0	0	0	0	0	1	8	1	0	0	0	1	0	0	1
1	0	0	0	1	0	0	1	0	9	1	0	0	1	1	0	1	0
2	0	0	1	0	0	0	1	1	10	1	0	1	0	1	0	1	1
3	0	0	1	1	0	1	0	0	11	1	0	1	1	0	0	0	0
4	0	1	0	0	0	1	0	1	12	1	1	0	0	X	X	X	X
5	0	1	0	1	0	1	1	0	13	1	1	0	1	X	X	X	X
6	0	1	1	0	0	1	1	1	14	1	1	1	0	X	X	X	X
7	0	1	1	1	1	0	0	0	15	1	1	1	1	X	X	X	X

Synchronous Counter

When counter is clocked such that each flip flop in the counter is triggered at the same time the counter is called as synchronous counter.

Design a 3-bit synchronous binary up-counter using IC 74x73 (JK-Flip Flop).

Step-1: Truth Table / Functional Table

PS			NS			FF Inputs					
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	1	1	0	x	0	1	x	x	1
1	1	0	1	1	1	x	0	x	0	1	x
1	1	1	0	0	0	x	1	x	1	x	1

Step-2: K-Map simplification

$\overline{Q_B} \overline{Q_A} \overline{Q_B} Q_A \overline{Q_B} Q_A \overline{Q_B} Q_A$

$\overline{Q_C}$	x	1	1	x
Q_C	x	1	1	x

$\overline{Q_B} \overline{Q_A} \overline{Q_B} Q_A \overline{Q_B} Q_A \overline{Q_B} Q_A$

$\overline{Q_C}$	x	x	1	0
Q_C	x	x	1	0

$$J_A = K_A = 1$$

$$K_B = Q_A$$

$\overline{Q_B} \overline{Q_A} \overline{Q_B} Q_A \overline{Q_B} Q_A \overline{Q_B} Q_A$

$\overline{Q_C}$	0	1	x	x
Q_C	0	1	x	x

$\overline{Q_B} \overline{Q_A} \overline{Q_B} Q_A \overline{Q_B} Q_A \overline{Q_B} Q_A$

$\overline{Q_C}$	x	x	x	x
Q_C	0	0	1	0

$\overline{Q_B} \overline{Q_A} \overline{Q_B} Q_A \overline{Q_B} Q_A \overline{Q_B} Q_A$

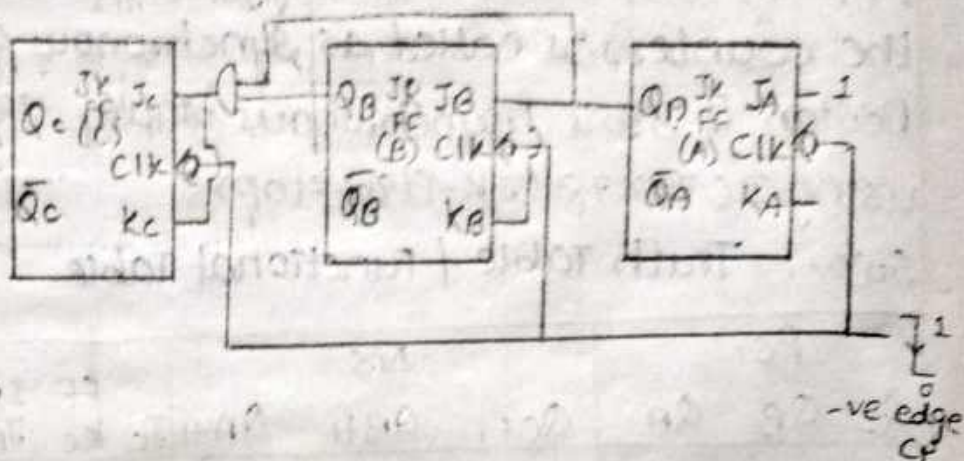
$\overline{Q_C}$	0	0	1	0
Q_C	x	x	x	x

$$J_B = Q_A$$

$$K_C = Q_B Q_A$$

$$J_C = Q_B Q_A$$

Step-3:- Logic diagram:



* For 4-bit synchronous up-counter $J_A = K_A = 1$
 $J_B = K_B = Q_A$ & $J_C = K_C = Q_A Q_B$ & $J_D = K_D = Q_A Q_B Q_C$
 Design MOD-7 synchronous up-counter by using T-Flip Flop.

Step-1:- Truth Table / Functional Table

PS			NS					
Q_C	Q_B	Q_A	Q_{CH}	Q_{BH}	Q_{AH}	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	0	0	0	1	1	0
1	1	1	X	X	X	X	X	X

Step-2:- k-Map simplification

$\overline{Q_B} \overline{Q_A} \overline{Q_C} \overline{Q_D} \overline{Q_E} \overline{Q_F} \overline{Q_G} \overline{Q_H}$

$\overline{Q_C}$	1	1	1	1
Q_C	1	1	X	0

$$T_A = \overline{Q_C} + \overline{Q_B}$$

$\overline{Q_B} \overline{Q_A} \overline{Q_C} \overline{Q_D} \overline{Q_E} \overline{Q_F} \overline{Q_G} \overline{Q_H}$

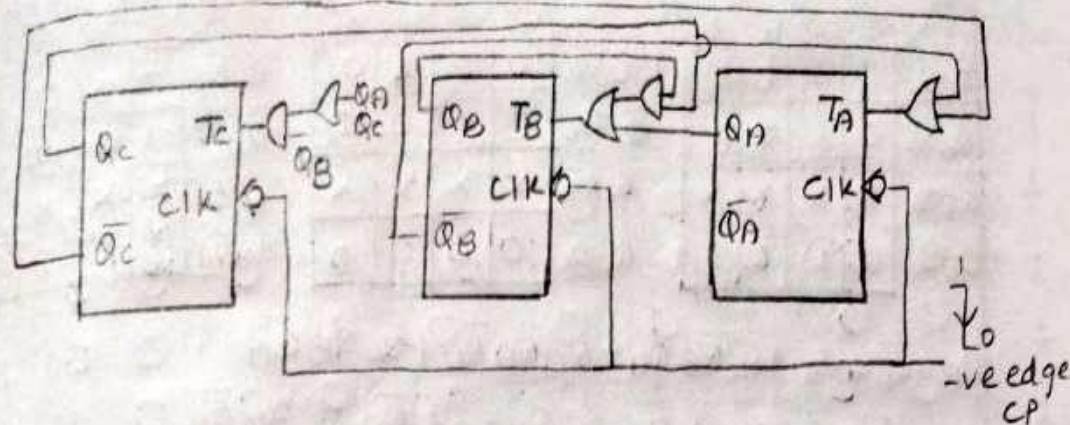
$\overline{Q_C}$	0	1	1	0
Q_C	0	1	X	1

$$T_B = Q_A + Q_C Q_B$$

$\overline{Q_B} \overline{Q_A} \overline{Q_C} \overline{Q_D} \overline{Q_E} \overline{Q_F} \overline{Q_G} \overline{Q_H}$

$\overline{Q_C}$	0	0	1	0
Q_C	0	0	X	1

$$T_C = Q_A Q_B + Q_B Q_C = Q_B (Q_A + Q_C)$$



Design divide by 12 synchronous up counter using IC 74x74.

Step-1:- Truth Table / Functional Table

PS				NLS							
QA	QC	QB	QA	QPH	QCH	QBH	QAH	TB	TC	TB	TA
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	0	1
1	0	1	1	0	0	0	0	0	0	0	0
1	1	0	0	X	X	X	X	X	X	X	X

Step-2:- K-Map simplification

$$Q_A = \overline{Q_B} \overline{Q_A} \overline{Q_D} + \overline{Q_C} \overline{Q_B} \overline{Q_A} + \overline{Q_C} Q_B \overline{Q_A} + \overline{Q_D} Q_B \overline{Q_A}$$

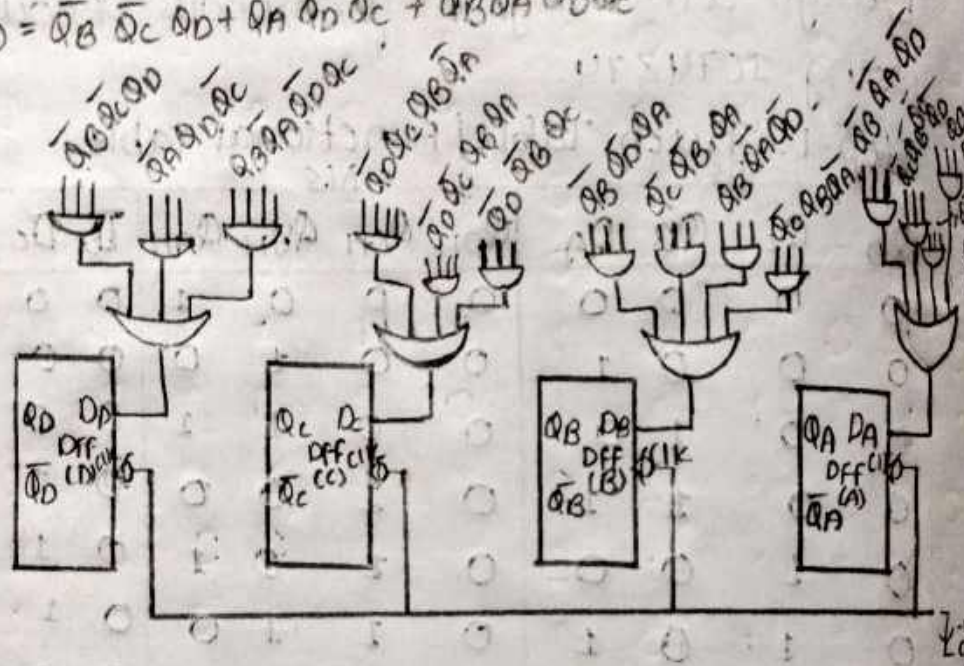
	$\overline{Q_B} \overline{Q_A}$	$\overline{Q_B} Q_A$	$Q_B \overline{Q_A}$	$Q_B Q_A$
$\overline{Q_D} \overline{Q_C}$	1	0	0	1
$\overline{Q_D} Q_C$	1	0	0	1
$Q_D \overline{Q_C}$	X	X	X	X
$Q_D Q_C$	1	0	0	1

$\overline{Q_D} \overline{Q_C} \overline{Q_B} \overline{Q_A}$	$\overline{Q_D} \overline{Q_C} Q_B \overline{Q_A}$	$\overline{Q_D} Q_C \overline{Q_B} \overline{Q_A}$	$\overline{Q_D} Q_C Q_B \overline{Q_A}$	$Q_D \overline{Q_C} \overline{Q_B} \overline{Q_A}$	$Q_D \overline{Q_C} Q_B \overline{Q_A}$	$Q_D Q_C \overline{Q_B} \overline{Q_A}$	$Q_D Q_C Q_B \overline{Q_A}$
0	0	0	0	0	0	0	0
0	1	0	0	0	1	0	0
1	1	1	1	1	1	1	1
0	1	0	1	0	1	0	1

$$D_B = \overline{Q_D} \overline{Q_C} Q_A + \overline{Q_D} Q_C \overline{Q_A} + Q_D \overline{Q_C} \overline{Q_A} + Q_D Q_C Q_A$$

$$D_C = \overline{Q_D} \overline{Q_B} Q_C + \overline{Q_D} Q_C Q_B Q_A + \overline{Q_D} Q_C Q_B \overline{Q_A}$$

$$D_D = \overline{Q_B} \overline{Q_C} Q_D + \overline{Q_A} Q_D \overline{Q_C} + Q_B \overline{Q_A} \overline{Q_D} Q_C$$



Design MOD-16 synchronous counter using TFF (4-bit counter) (Divide by 16)

Step-1:- Functional Table / Truth Table

Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_D	T_C	T_B	T_A
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1

Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_D	T_C	T_B	T_A
1	0	0	1	1	0	1	0	0	0	1	1
1	0	1	0	1	0	1	1	0	0	0	1
1	0	1	1	1	1	0	0	0	1	1	1
1	1	0	0	1	1	0	1	0	0	0	1
1	1	0	1	1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1	0	0	0	1
1	1	1	1	0	0	0	0	1	1	1	1

K-Map simplification (Step-2):

$$T_A = 1$$

T_B

	$Q_B Q_A$	$\bar{Q}_B Q_A$	$Q_B \bar{Q}_A$	$\bar{Q}_B \bar{Q}_A$
$Q_D \bar{Q}_C$	0	1	1	0
$\bar{Q}_D \bar{Q}_C$	0	1	1	0
$Q_D Q_C$	0	1	1	0
$\bar{Q}_D Q_C$	0	1	1	0

T_C

	$Q_B Q_A$	$\bar{Q}_B Q_A$	$Q_B \bar{Q}_A$	$\bar{Q}_B \bar{Q}_A$
$Q_D \bar{Q}_C$	0	0	1	0
$\bar{Q}_D \bar{Q}_C$	0	0	1	0
$Q_D Q_C$	0	0	1	0
$\bar{Q}_D Q_C$	0	0	1	0

T_D

	$Q_B Q_A$	$\bar{Q}_B Q_A$	$Q_B \bar{Q}_A$	$\bar{Q}_B \bar{Q}_A$
$Q_D \bar{Q}_C$	0	0	0	0
$\bar{Q}_D \bar{Q}_C$	0	0	1	0
$Q_D Q_C$	0	0	1	0
$\bar{Q}_D Q_C$	0	0	0	0

$$T_B = Q_A$$

$$T_C = Q_B Q_A$$

$$T_D = Q_C Q_B Q_A$$

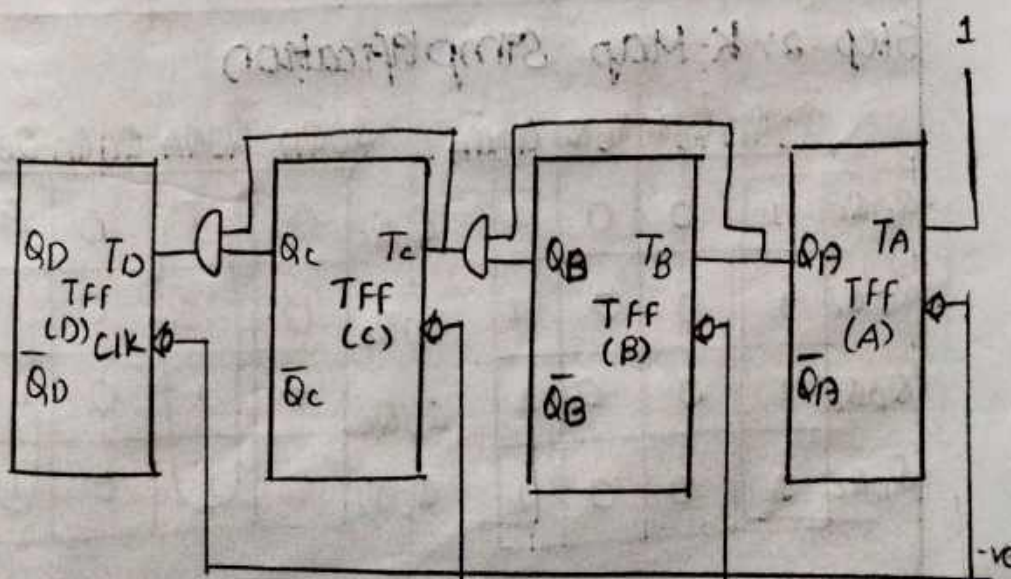


Fig:- Design of MOD-16 synchronous Up counter using TFF

CLK pulse

Design a 4-bit Synchronous Counter using 74x74

Step-1: Functional Table:-

Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}	D_D	D_C	D_B	D_A
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1
0	0	1	0	0	0	1	1	0	0	1	0
0	0	1	1	0	1	0	0	0	0	1	1
0	1	0	0	0	1	0	1	0	1	0	0
0	1	0	1	0	1	1	0	0	1	0	1
0	1	1	0	0	1	1	1	0	1	1	0
0	1	1	1	1	0	0	0	0	1	1	1
1	0	0	0	1	0	0	1	1	0	0	0
1	0	0	1	1	0	1	0	1	0	0	1
1	0	1	0	1	0	1	1	1	0	1	0
1	0	1	1	1	1	0	0	1	1	0	1
1	1	0	0	1	1	0	1	1	1	0	0
1	1	0	1	1	1	1	0	1	1	0	1
1	1	1	0	1	1	1	1	1	1	1	0
1	1	1	1	0	0	0	0	0	0	0	0

Step-2: K-Map Simplification

$\bar{Q}_B \bar{Q}_A \bar{Q}_B Q_A \bar{Q}_B \bar{Q}_A \bar{Q}_B Q_A$

$\bar{Q}_D \bar{Q}_C$	1	0	0	1
$\bar{Q}_D Q_C$	1	0	0	1
$Q_D \bar{Q}_C$	1	0	0	1
$Q_D Q_C$	1	0	0	1

$\bar{Q}_B \bar{Q}_A \bar{Q}_B Q_A \bar{Q}_B \bar{Q}_A \bar{Q}_B Q_A$

$\bar{Q}_D \bar{Q}_C$	0	1	0	1
$\bar{Q}_D Q_C$	0	1	0	1
$Q_D \bar{Q}_C$	0	1	0	1
$Q_D Q_C$	0	1	0	1

$$D_A = \bar{Q}_A$$

$$D_B = Q_B \bar{Q}_A + \bar{Q}_B Q_A$$

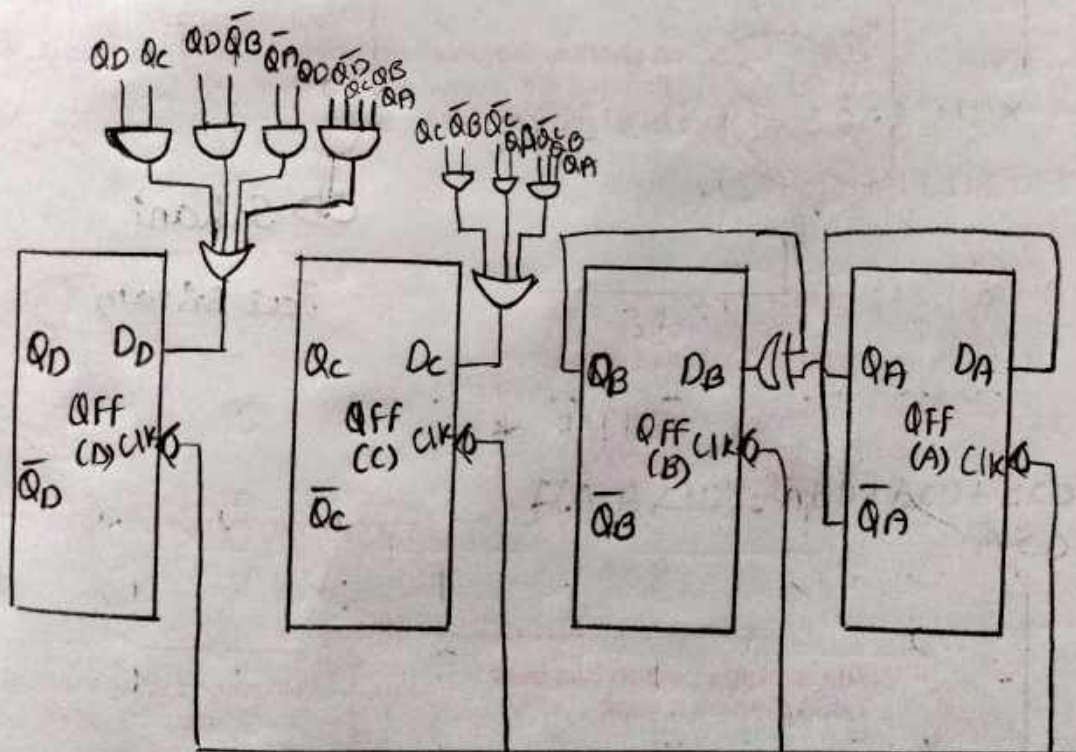
$$= Q_A \oplus Q_B$$

	$\bar{Q}_B \bar{Q}_A$	$\bar{Q}_B Q_A$	$Q_B \bar{Q}_A$	$Q_B Q_A$
$\bar{Q}_D \bar{Q}_C$	0	0	1	0
$\bar{Q}_D Q_C$	1	1	0	1
$Q_D \bar{Q}_C$	1	1	0	1
$Q_D Q_C$	0	0	1	0

$$D_C = Q_C \bar{Q}_B + \bar{Q}_C Q_B Q_A + \bar{Q}_A Q_C$$

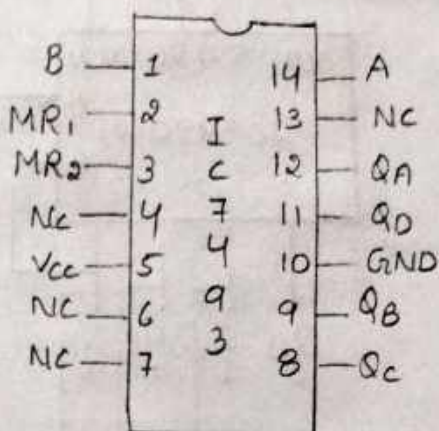
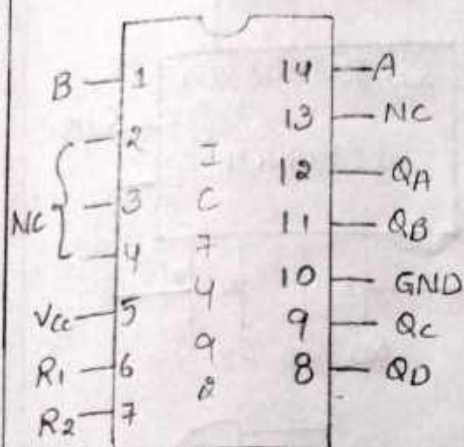
	$\bar{Q}_B \bar{Q}_A$	$\bar{Q}_B Q_A$	$Q_B \bar{Q}_A$	$Q_B Q_A$
$\bar{Q}_D \bar{Q}_C$	0	0	0	0
$\bar{Q}_D Q_C$	0	0	1	0
$Q_D \bar{Q}_C$	1	1	0	1
$Q_D Q_C$	1	1	1	1

$$D_D = Q_D \bar{Q}_C + Q_D \bar{Q}_B + \bar{Q}_A Q_D + \bar{Q}_D Q_C Q_B Q_A$$

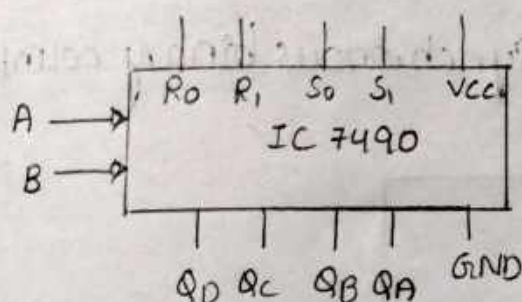


7-ve
CP

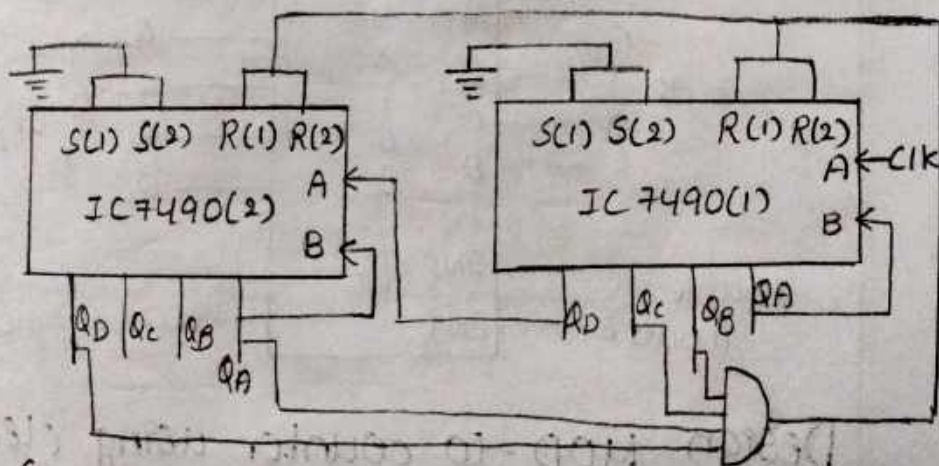
Design 4-bit Ripple Counter (IC 7492/7493)



Decade Counter (IC 7490)



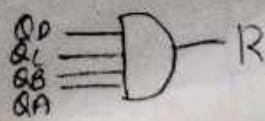
Design Divide by 96 counter using IC 7490.

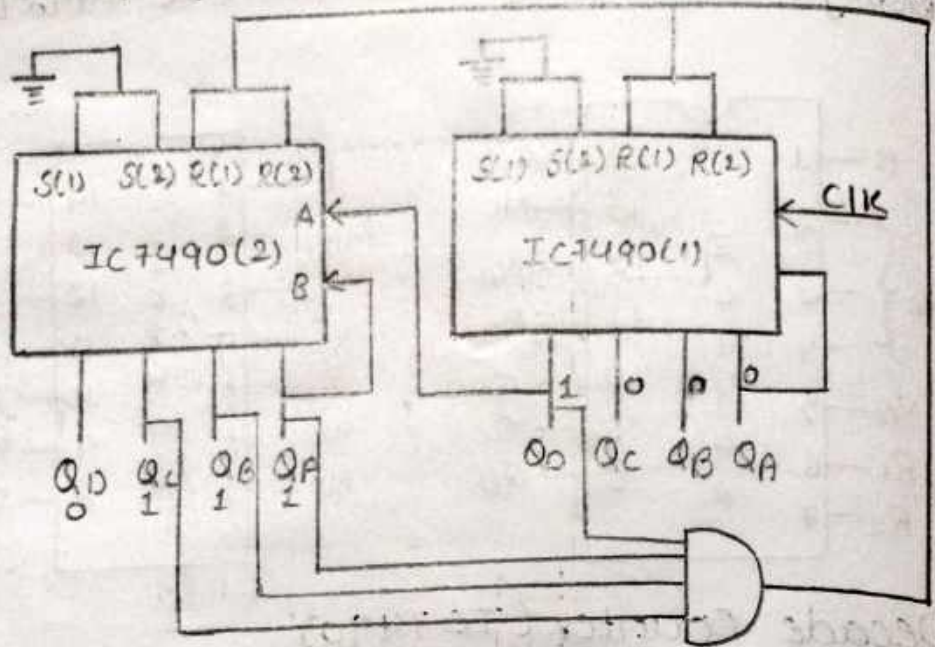


9 6
| |
1001 0110

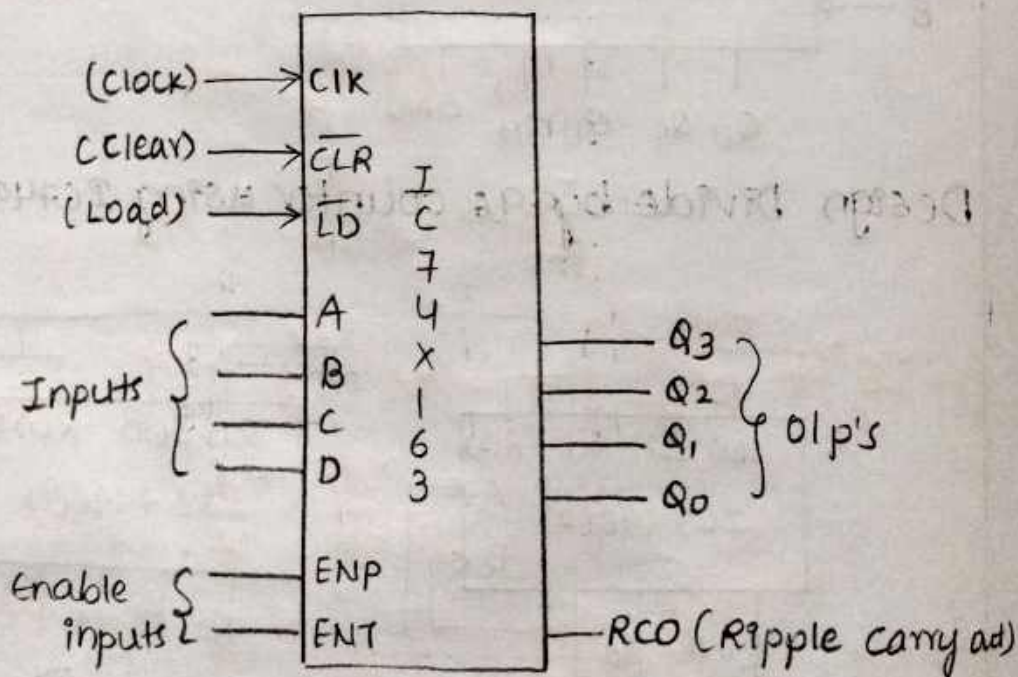
Design Divide by 78 counter using IC 7490.

7 8
| |
0111 1000





IC 74163 (4-bit Synchronous binary counter)

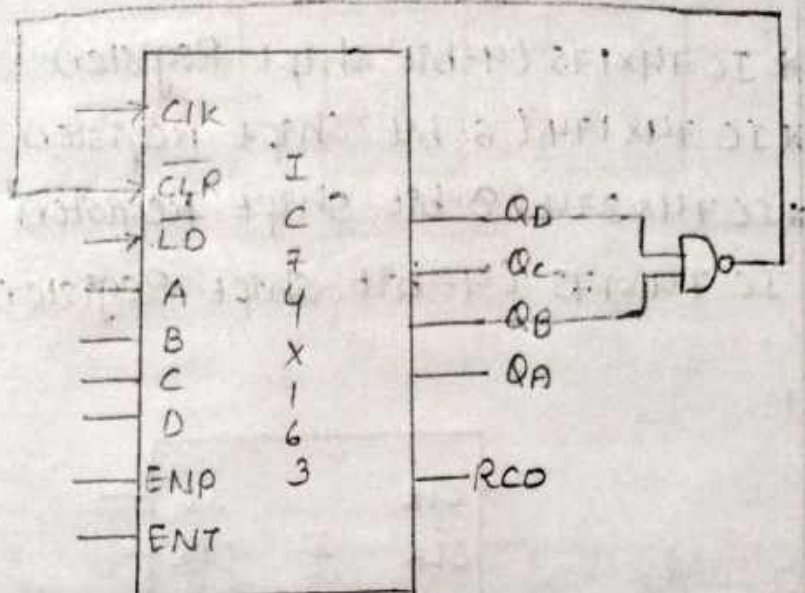


Design MOD-10 counter using clear input

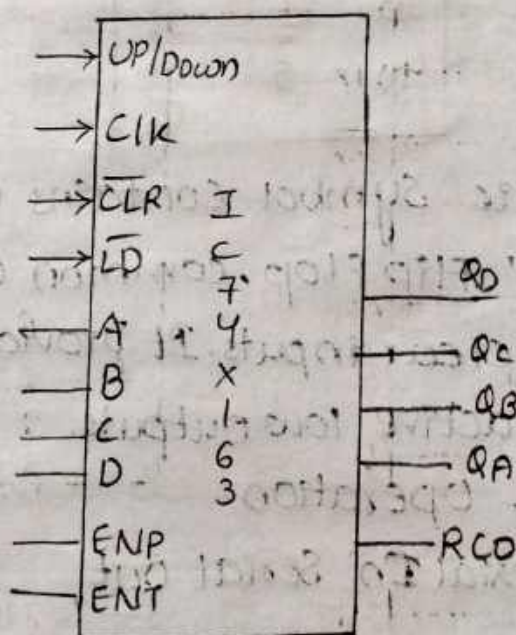
10

↳ In Binary

1010
Q_D Q_C Q_B Q_A



4-bit Bidirectional synchronous counter



Shift Register

Shift Registers are used to shift the data serially and parallelly

1. SISO
2. SIPO
3. PISO
4. PIPO

5. Bidirectional Shift Register

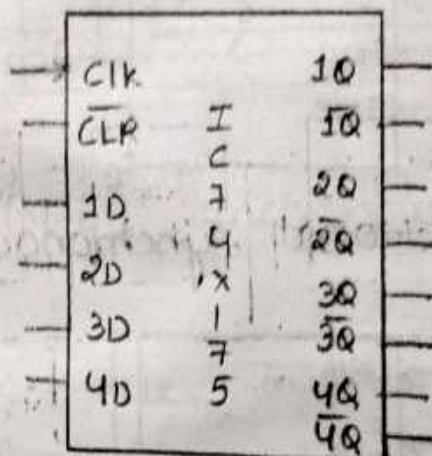
6. Universal Shift Register

* IC 74x175 (4-bit shift Register)

* IC 74x174 (6-bit shift Register)

* IC 74x374 (8-bit shift Register)

IC 74x175 (4-bit shift Register)



This logic symbol contains 4 negative edge trigger 'D' Flip Flop, common clock and asynchronous clear inputs. It provides both active high and active low outputs.

Modes of Operation

1. SISO - Serial In Serial Out

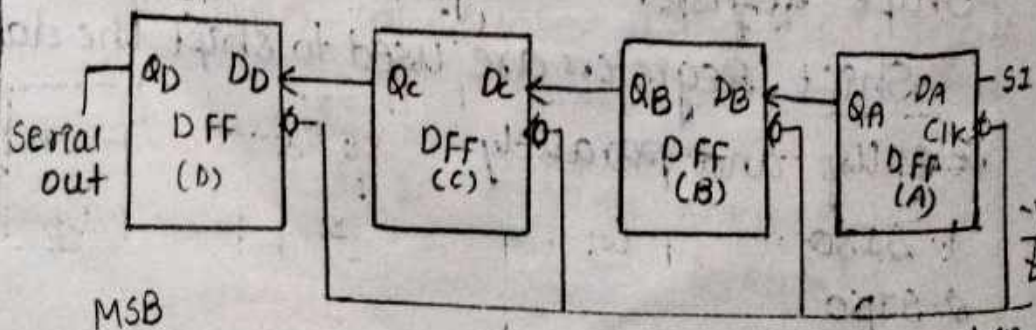


Fig:- SISO (Shift left) shift Register

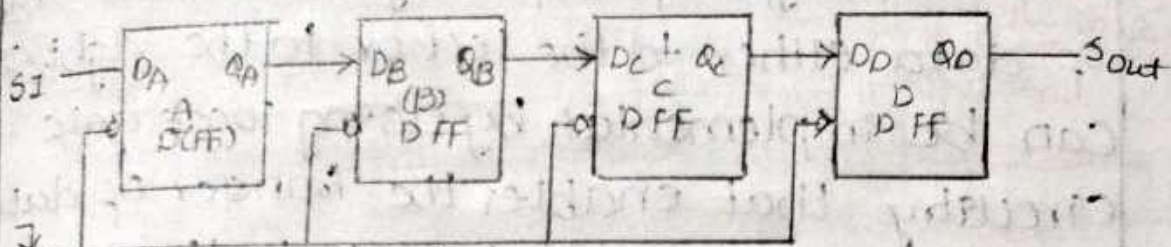
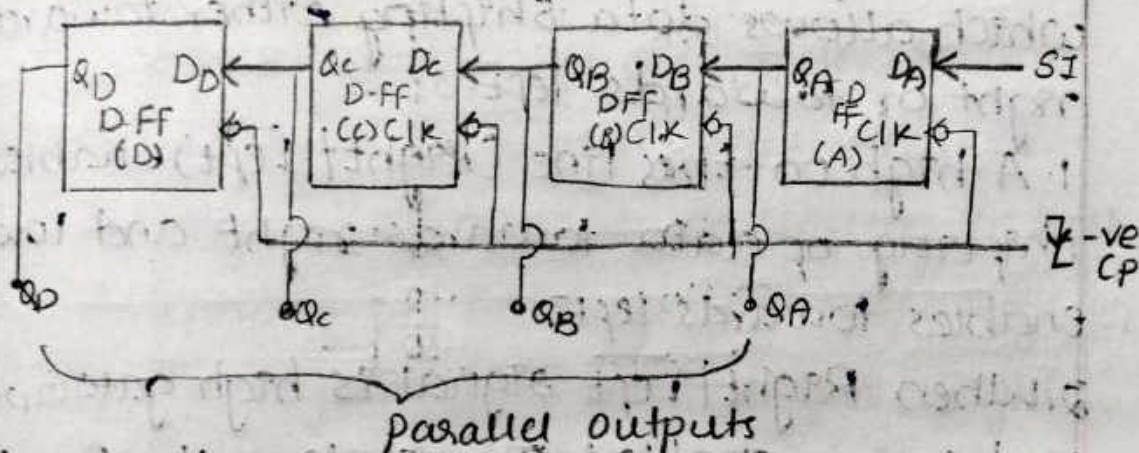
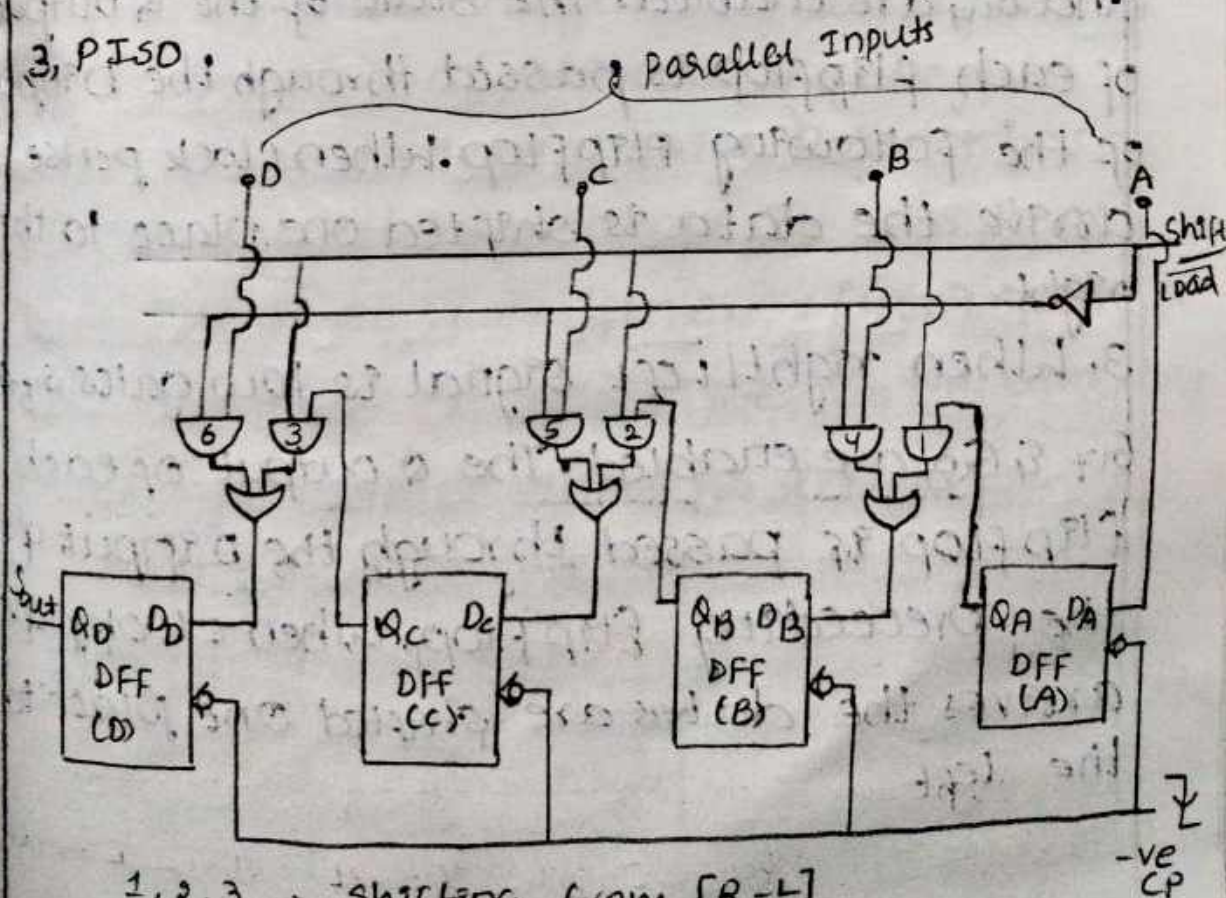


Fig :- SISO. (Shift Right) Shift Register

8, SIPO



3, PISO



1, 2, 3 → Shifting from [R-L]

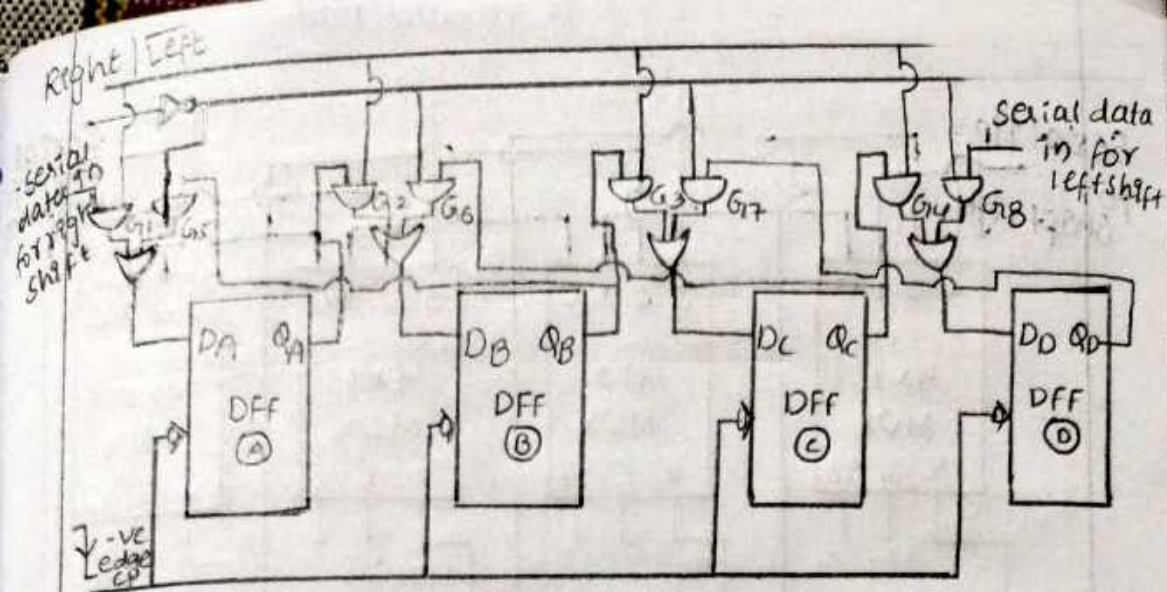
4, 5, 6 → To load the data parallelly

4) Bidirectional Shift Register

This type of shift Register allows shifting of data either to the left or to the right. It can be implemented by using logic gate circuitry that enables the transfer of data from one state to next state to the right or to the left depending upon the level of control lines.

The Right/Left is the control input signal which allows data shifting either towards right or towards left.

1. A high on this line (Right/Left) enables the shifting of data towards right and low enables towards left.
2. When Right/Left signal is high gates G_1, G_2, G_3 and G_4 are enabled. The state of the Q output of each flipflop is passed through the D input of the following flipflop. When clock pulse arrives the data is shifted one place to the right.
3. When right/Left signal is low gates G_5, G_6, G_7 & G_8 are enabled. The Q output of each flipflop is passed through the D input of the preceding flipflop. When clock pulse arrives the data is shifted one place to the left.



Universal shift Register

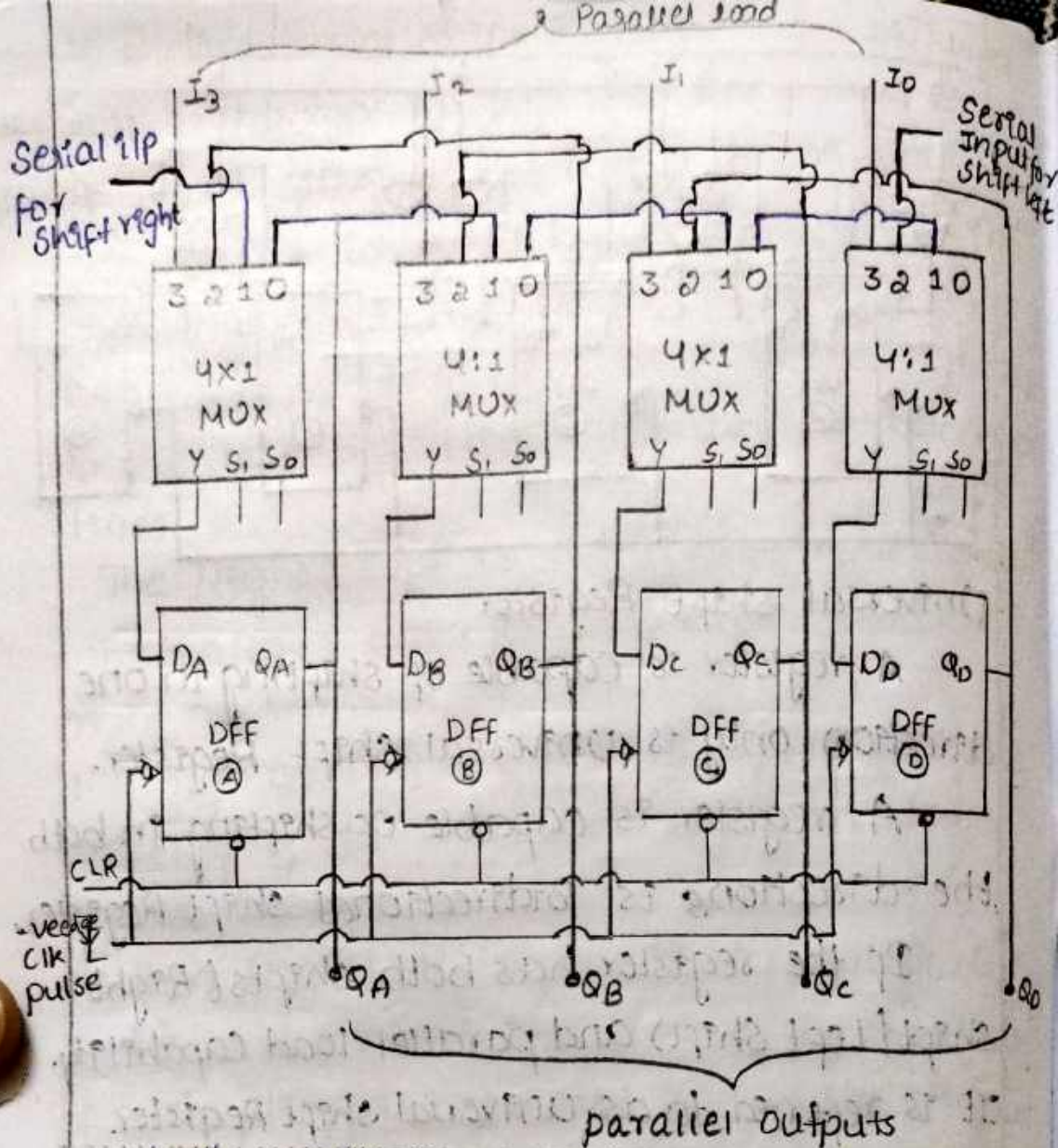
A register is capable of shifting in one direction only is Universal Shift Register.

A register is capable of shifting in both the directions is Bidirectional Shift Register.

If the register has both shifts (Right shift / Left shift) and parallel load capability. It is referred to as Universal Shift Register.

A 4-bit Universal Shift Register has all the capabilities listed above. It consists of four flip flops, 4 multiplexers (4:1), 4:1 Mux has two common select lines S_0 and S_1 , and they select appropriate input for D Flip Flop.

Mode Control	Register operation
S_1 S_0	
0 0	No change
0 1	Shift Right
1 0	Shift Left
1 1	Parallel loading



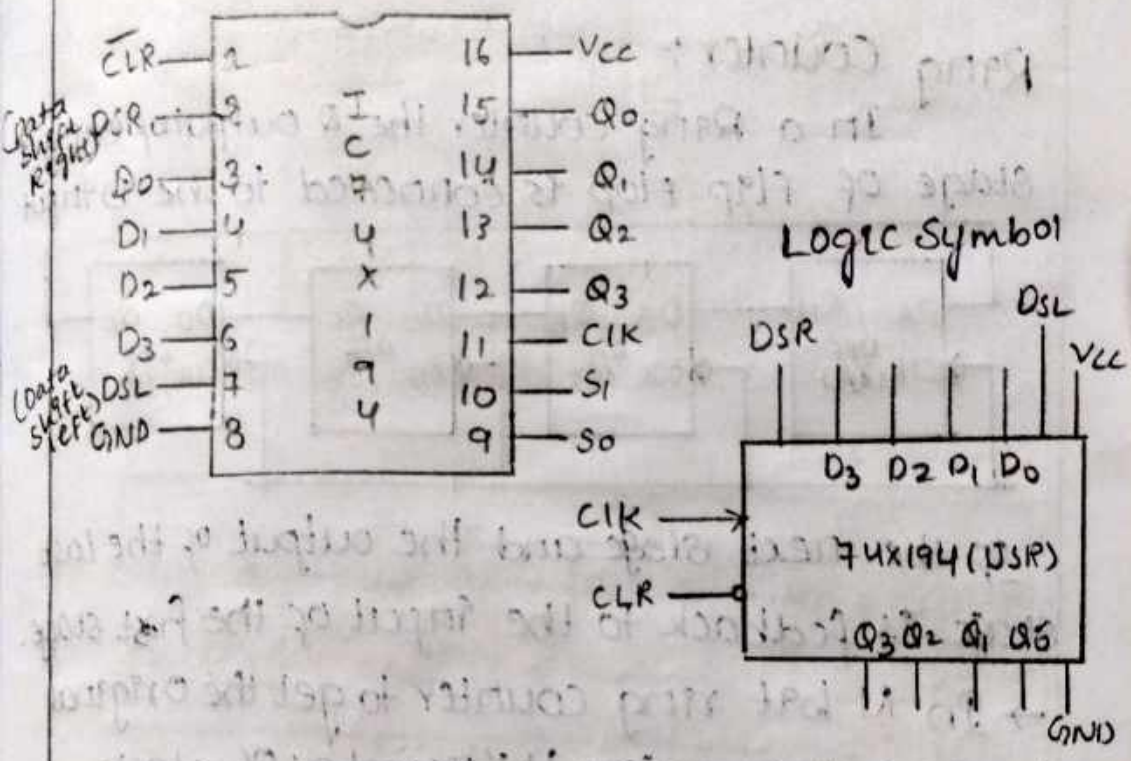
The table shows the register operation depending on the select inputs of the MUX.

- 1) When $S_1 \& S_0 = 0$, the input '0' is selected and the present value of the register is applied to the D inputs of the Flip Flop. This results in no change in the register value.
- 2) When $S_1 = 0 \& S_0 = 1$, input '1' is selected and the circuit connections are such that it operates as a Right shift operation.
- 3) When $S_1 = 1 \& S_0 = 0$, the input '2' is selected and the circuit connections are such that

it operates as a left shift Register.

4) Finally $S_1=1$ & $S_0=1$ the binary information on the parallel input line transferred into the Register simultaneously and it is a parallel load operation

IC 74x194 (Universal Shift Register)



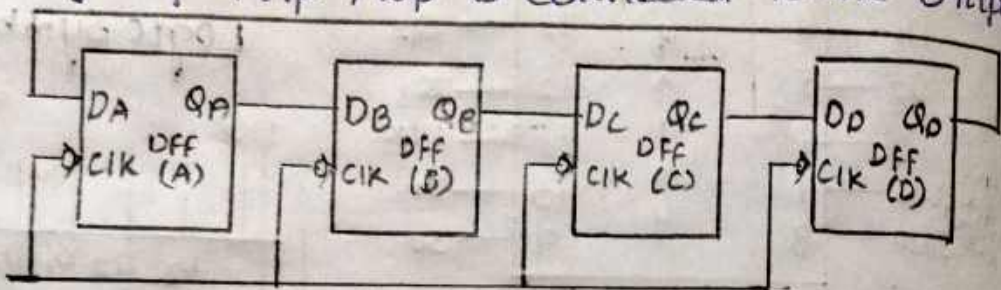
Operation Mode	Inputs							Outputs			
	CLK	$\overline{\text{CLR}}$	S_1	S_0	DSR	DSL	D_0	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	0	X	X	X	X	X	0	0	0	0
Shift-left	↑	1	1	0	X	0	X	Q_1	Q_2	Q_3	0
	↑	1	1	0	X	1	X	Q_1	Q_2	Q_3	1
Shift-Right	↑	1	0	1	0	X	X	0	Q_0	Q_1	Q_2
	↑	1	0	1	1	X	X	1	Q_0	Q_1	Q_2
Parallel load	↑	1	1	1	X	X	D_0	D_0	D_1	D_2	D_3
Hold mode	X	1	0	0	X	X	X	Q_0	Q_1	Q_2	Q_3

Applications of Shift Registers:-

- * With the help of shift Register we can shift the data serially, parallelly in shift-left, shift-Right Mode (SISO, SIPO, PISO, PPO, Universal SR, Bidirectional SR).

Ring Counter:-

In a Ring counter the Q output of each stage of Flip Flop is connected to the D input

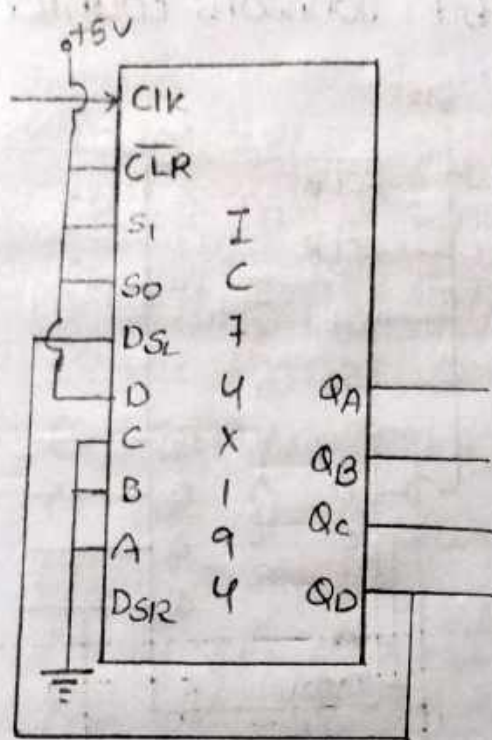


of the next stage and the output of the last stage is feedback to the input of the first stage.

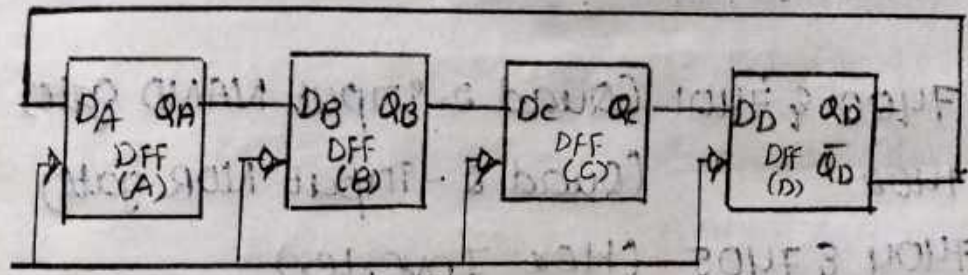
→ In N bit ring counter to get the original (initial) information, 'N' number of clock pulses are needed.

For example: For a 4-bit ring counter it needs a 4-clock pulses to get initial information.

Design a 4-bit ring counter using IC 74194

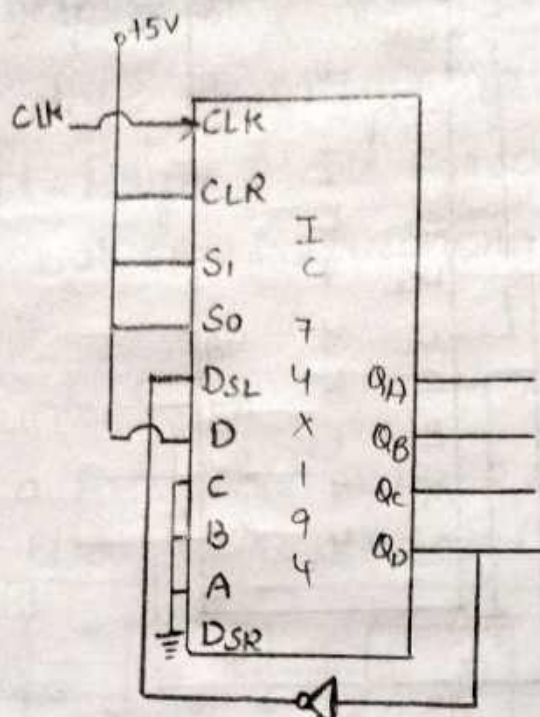


Twisted Ring Counter:-



Q ₁	Q ₂	Q ₃	Q ₄	CP
0	0	0	1	0
0	0	0	0	1
1	0	0	0	2
1	1	0	0	3
1	1	1	0	4
1	1	1	1	5
0	1	1	1	6
0	0	1	1	7
0	0	0	1	8

Design a 4-bit Johnsons counter using
74X194



- ✓ 7400 & 7401 (Quad 2-input NAND gate)
- ✓ 7402 (Quad 2-input NOR gate)
- 7404 & 7405 (Hex Inverter)
- 7408 & 7409 (Quad 2-input AND gate)
- 7432 (Quad 2-input OR gate)
- 74135 (Quad Ex-OR gate)
- 74136 (Quad 2-input Ex-OR gate)
- ✓ 7446, 7447 & 7449 (BCD to 7 segment decoder)
- 7442 (BCD to Decimal Decoder)
- ✓ 74148 (Priority Encoder) (Octal to Binary Converter)
- 74157, 74158 (Quad 2:1 MUX)
- 74153 (Quad 4:1 MUX)
- ✓ 74151 (8:1 MUX)

- ✓ 74150 (16:1 Mux)
- ✓ 74138 (3:8 decoder) (1:8 DE-Mux)
- ✓ 74139 (dual 2:4 decoder) (dual 1:4 DE-Mux)
- 74180 (8-bit Parity Generator)
- ✓ 74280 (9-bit Parity Generator)
- ✓ 7483 (4-bit Parallel Adder / 4-bit Full adder)
- ✓ 7485 (4-bit Comparator)
- ✓ 74LS182 (Look-Ahead Carry Generator)
- ✓ 74x74 (Dual D-Flip Flop)
- ✓ 74x73 (Dual JK-Flip Flop)
- ✓ 7490 (Decade code counter / BCD counter)
Mod-10 counter
- 7493 (4-bit Binary Ripple Counter /
Asynchronous counter)
- 74163 (4-bit Binary Synchronous / parallel
counter)
- 74168 & 74169 (4-bit Up/down Synchronous
counter)
- 7494 (4-bit Shift Register)
- 7491 (8-bit Shift Register)
- 74194 (4-bit Universal Shift Register)

Memories:-

Memories

ROM

(Read Only Memory)
(Non-volatile)

RAM (RWM)

(Random Access
Memory)
(Volatile)

Types of ROM

1. MROM (Mask ROM)
2. PROM (Programmable ROM)
3. EPROM (Electrically Programmable ROM)
(UVPROM - Ultra Violet Programmable ROM)
4. EEPROM (Electrically Erasable Programmable ROM)

Types of RAM :-

1. SRAM (Static RAM) (1T, 6T)
2. DRAM (Dynamic RAM) (1T, 3T)

ROM (Read Only Memory) :-

By using ROM we can't write data into the memory and only we can read the information from the memory.

It is a Non-volatile memory that is it can hold data even if power is turned off.

Generally ROM is used to store binary codes for the sequence of instructions given and data such as look up tables. This type of information does not change. There are 4 types of ROM.

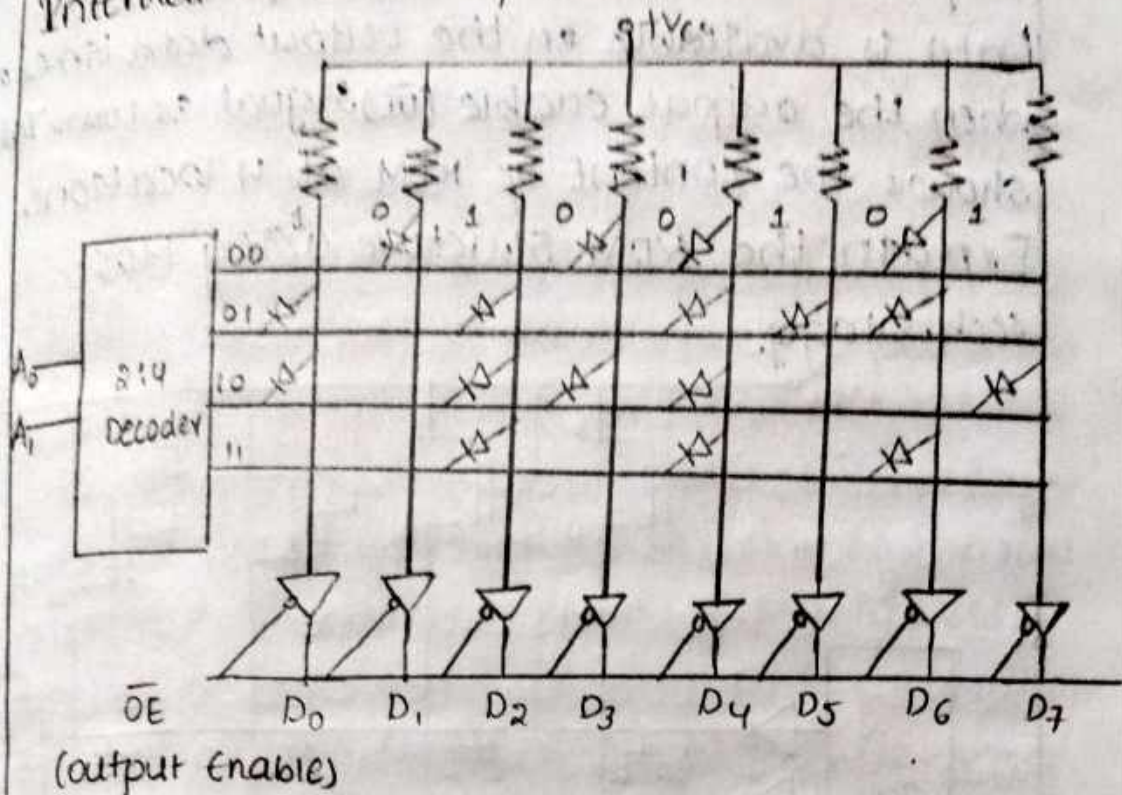
1) MROM

4) EEPROM

2) PROM

3) EPROM

Internal structure of ROM:-



Address in Binary	Binary data								Data in Hexadecimal
	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	
0 0	1	0	1	0	0	1	0	1	A 5
0 1	0	1	0	1	0	0	0	1	5 1
1 0	0	1	0	0	0	1	1	0	4 6
1 1	1	1	0	1	0	1	0	1	D 5

Fig:- Table Content of ROM

A Figure Shows a simple 4-byte diode ROM. Diode ROM consists of only diodes and decoders. Address lines A_0 & A_1 are decoded by 2:4 decoder and are used to select one of the four rows. As the decoder output is active low it places a logic '0' on the selected row. Each output data line goes to logic 0 if a diode connects the

Output data column to the selected row. Data is available on the output data lines only when the output enable ($\overline{OE}$) signal is low. Table shows the content of ROM at 4 locations. Explain the ROM structure using Mos technology.

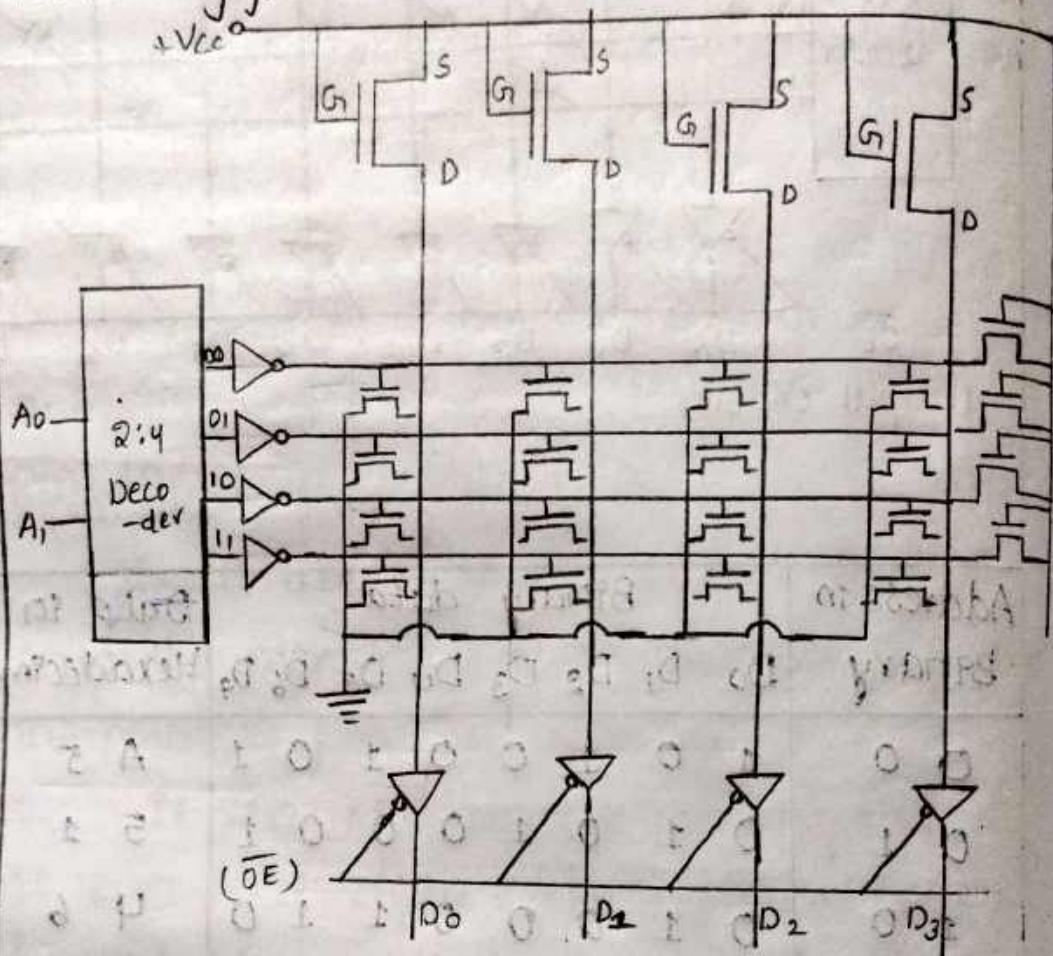


Fig:- Sample 4 Nibble (Half byte) MOS ROM

Now a days ROM use Mos technology instead of Diode. Figure shows Four Nibble (Half byte) ROM using Mos transistor. Here diodes and Pull up resistors are replaced by Mos transistor. The address on the address line (A_0-A_2) is decoded by 2:4 Decoder
 → Decoder selects one of the four rows

by making it logic '0'. The inverter connected at the output of the decoder inverts at the selected row (logic 1) therefore each output data line goes to logic 0 if the gate of the MOS transistor connected to row select lines.

→ When gate of MOS transistor is connected to selected row. MOS transistor is turned ON. This pulls the corresponding column data line to logic '0'.

→ In Integrated circuit a thin metalized layer connects the gate of some transistor to the row select line. The gate connection of MOS transistor depends on the data to be store in the ROM. Therefore according to the users truth table, manufacturer can deposit thin layer of metal to connect gate of the transistor. Such ROM are called MOS programmed ROMs.

These are used in Microprocessor based toys, TV, games, Home computers, etc. ---

Explain the necessity of two dimensional decoding mechanism in memories MOS transistor memory cell in ROM Operation.

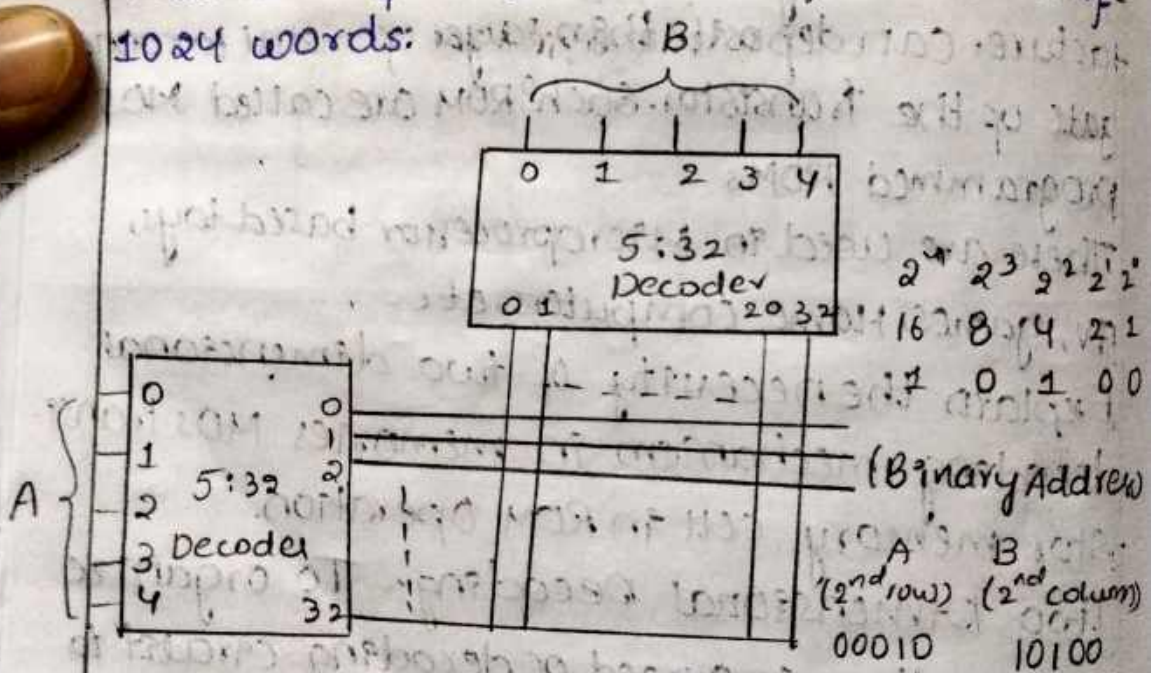
Two Dimensional Decoding:- To organize memory there is a need of decoding circuit to select the memory word specified by the input address.

The two-dimensional selection pattern is shown in figure. It has $n=10$ i.e., 10 decoder inputs.

These decoder inputs are divided by 2 to get individual decoding inputs i.e., 5 inputs for

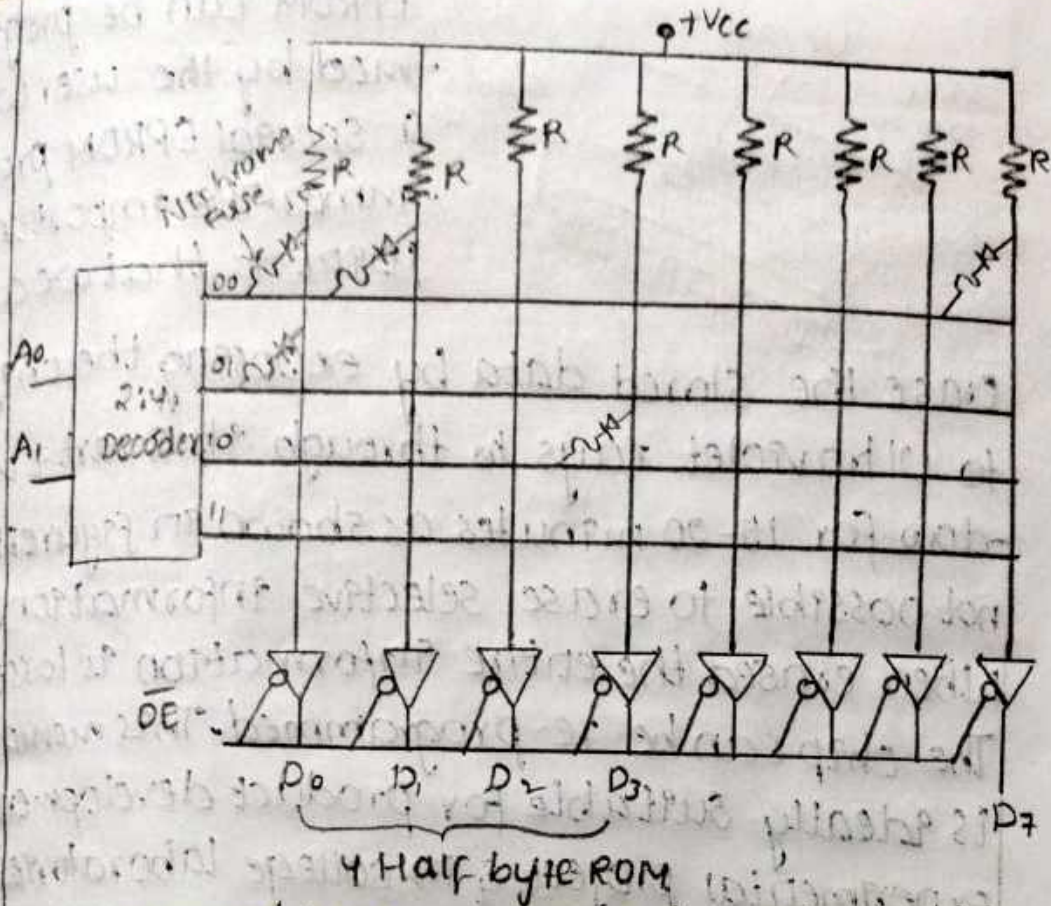
each decoder. Therefore instead of using 10×1024 ($n: 2^n$) we use 2 5×32 decoder. ^{single AND}
 a single decoder we would need 1024 ^{AND} gates with 10 inputs in each.

In Two decoder case, we need 64 AND gates with a 5 inputs in each. The 5 MSB of the address go to input A & 5 LSB of the bits go to input B. Each word input within the memory array is selected by the coincidence of 1A & 1B line. Thus each ~~line~~ word in memory is selected by the coincidence between 1:32 rows & 1:32 columns for a total of 1024 words.



PROM (Programmable ROM):

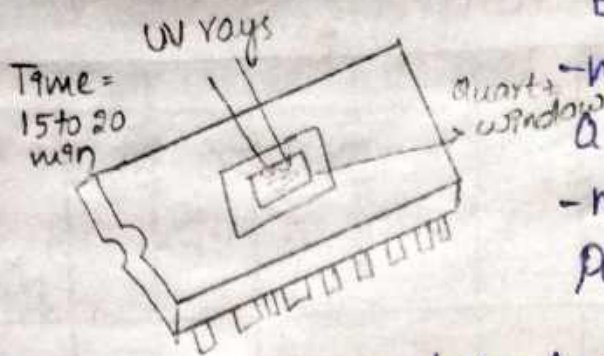
Figure shows 4 byte ROM. It has diodes in every bit position therefore output is initially all zeros. Each diode has a fusible link in series with it. By addressing bit and applying proper pulse current pulse at the corresponding output we can glow out the



fuse storing logic 1 at that position. The fuse uses material like Nixchrome (or) poly crystalline material. For blowing the Fuse it is necessary to pass around 20-50 amp of current for a period of 5-20 μ sec. The blowing of fuses according to the truth table is called programming of ROM. The user can program PROM's with a special PROM programmer. The PROM programmer selectively burns the fuses according to the bit pattern to be stored. This process is also known as burning of PROM. The PROMs are one time programmable. Once programmed the information stored is permanent.

EPROM (Erasable Programmable ROM):

It uses MOS circuitry. They store 1 's as a packet of charge in the IC chip.



EPROM can be programmed by the user with a special EPROM programmer. The important point is that we can

erase the stored data by exposing the chip to ultraviolet rays through its quartz window for 15-20 minutes as shown in figure. It is not possible to erase selective information.

When erased the entire information is lost. The chip can be re-programmed. This memory is ideally suitable for product development, experimental project & in college laboratories.

Since this chip can be reused many times.

During programming, address and data are applied to address and data to the EPROM.

EEPROM (Electrically Erasable Programmable Read Only Memory):

EEPROM also uses MOS circuitry very similar to that of EPROM. Data is stored as a charge or no charge on an insulated layer. The insulating layer made very thin. Therefore the voltage as low as 5V can be used to move charges across the thin layer in either direction for programming or erasing.

→ It allows selective erasing at the ^{cell} level rather than erasing all the information since the information can be erase by using

electrical signals.

→ It also has special erase mode by which entire chip can be erase in 10msec.

→ This time is quite small as compared to time required to erase EPROM and it can erase and reprogram the device right in the circuit.

Disadvantage:-

* Most Expensive

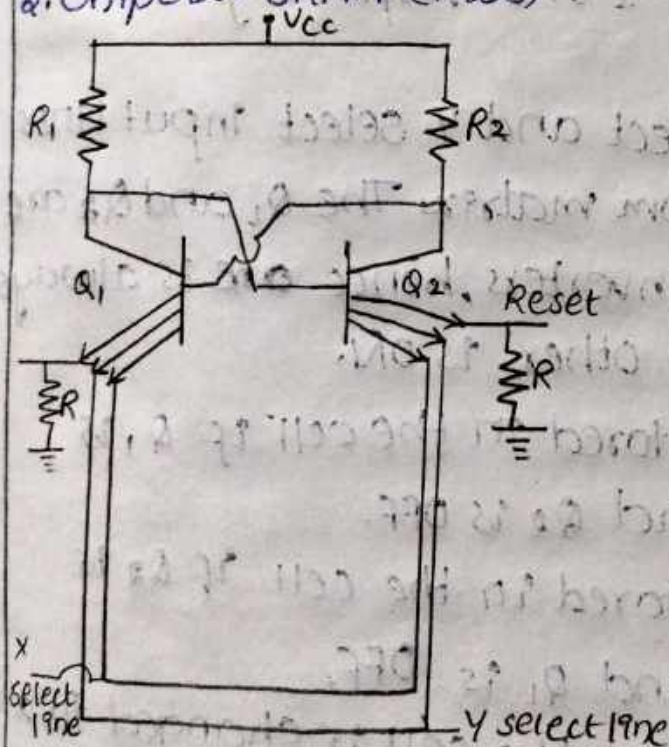
* Least Dense ROM (easy breakables)

RAM (Random Access Memory) (RWIM):-

SRAM (Static RAM):-

1. Bipolar SRAM (TTL)

2. Unipolar SRAM (MOS)



T1R RAM cell

Memories that consists of circuits capable of retaining their state as long as power is applied are known as static memories.

These are Random Access Memory (RAM) and hence combinely called Static RAM memories. Most of the static RAMs are built using MOS technology but some are built using bipolar technology.

Bipolar RAM:-

Figure shows a simplified schematic of bipolar memory cell. The memory cell is implemented using TTL (Transistor - Transistor Logic) multiple emitter technology. It stores 1 bit of information. It is nothing but a Flip-flop. It can store either 0 or 1, as long as power is applied, and it can set or reset to store either 1 or 0 respectively.

Operation:-

The X select and Y select input lines select a cell from matrix. The Q_1 and Q_2 are cross coupled inverters, hence one is always OFF while the other is ON.

A "1" is stored in the cell if Q_1 is conducting and Q_2 is OFF.

A "0" is stored in the cell if Q_2 is conducting and Q_1 is OFF.

The state of the cell is changed to a "0" by pulsing a HIGH on the Q_1 (SET) emitter. This turns off Q_1 , when Q_1 is turned off, Q_2 is turned on.

As long as Q_2 is ON, its collector is low

and Q_1 is held OFF.

A 1 can be rewritten by pulsing the Q_2 (reset) emitter HIGH.

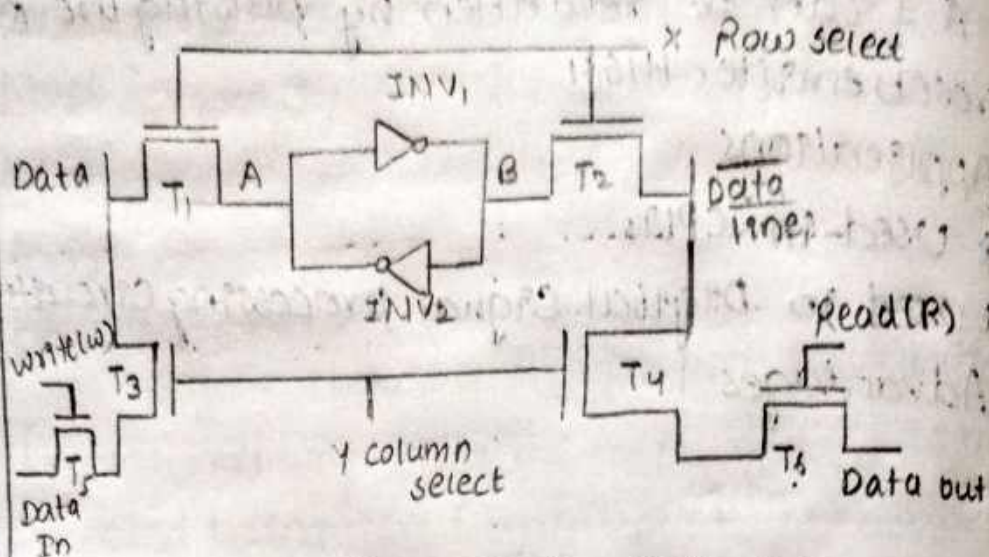
Applications

* Used in CPUs.

* Used in Digital Signal Processing Circuits.

Advantages

MOSFET SRAM Cell:-



Mos Static RAM Cell

Enhancement MOSFET transistors are used to make this RAM cell. X and Y are used for addressing the cell. When X & Y both are high, cell is selected.

* When $X=1$, T_1 & T_2 get ON, and the cell is connected to the data line & data line.

* When $Y=1$, T_3 & T_4 are made ON. Due to this, either read or write operation is possible.

Write Operation

Write Operation can be enabled by making w signal high, with write operation enabled, if data-in signal is logic 1, node A is also logic 1 & node B is at logic 0.

If $w=1$, Data=0, node A=0 & node B=1

Read Operation

Read operation can be enabled by making R signal high, with read operation enabled, T_6 becomes ON. This connects the

data output line to the data out and thus complement of the bit stored in the cell is available at the output.

Differences between RAM & ROM:-

RAM	ROM
1. Full form of RAM is Random Access Memory (or) RWM (Read write Memory)	1. Full form of ROM is Read only Memory.
2. RAM is volatile memory.	2. ROM is Non-volatile Memory.
3. RAM is expensive compared to ROM.	3. ROM is cheaper in comparison to RAM.
4. Data in RAM can be modified, read or erased.	4. Data in ROM can only be Read.
5. RAM is temporary storage.	5. ROM is permanent storage.
6. Writing data on RAM is faster than ROM.	6. Writing data on ROM is slower.
7. RAM can be accessed by the CPU directly.	7. The data of ROM needs to be transmitted to RAM to give access to the CPU to its data.
8. Stored data in Mega bits (MBs)	8. Stored data in Giga bits (GBs)

RAM

9. Larger size with high capacity.
10. Very fast but uses a lot of power

ROM

9. small size with less capacity.
10. Fast but uses very little power.

Comparison between Static RAM & Dynamic RAM.

SRAM

1. Static RAM chip contains a large number of flipflops which are basic memory cells. The Flip Flop comprise of bipolar transistors.
2. The Access time is less (a few tens of ns) hence faster memory.
3. Chip density is less.
4. Refreshing of the memory chip is not necessary. Hence no extra hardware is needed. System design is simple.

DRAM

1. Dynamic RAM chip contains a large number of basic cells. Each logic cell comprising of a MOSFET and a capacitor data is stored as charges on the capacitor.
2. The Access time is more (a few hundreds of ns).
3. Chip density is more.
4. Since data is stored as charge on capacitor very frequent refreshing of the chip is absolutely essential. Hence extra hardware is needed. System design is complex.

SRAM

- 5. Less power dissipation
- 6. Cost of SRAM chip is less.

DRAM

- 5. High power dissipation
- 6. Cost of DRAM chip is high.

Dynamic RAM:-

Dynamic RAM uses an entirely different technology as compared to static RAM. Where as in static RAM data is stored in Flip-Flops, in dynamic RAM, data is stored as charge on Capacitors. A basic dynamic RAM cell is shown in figure.

A basic cell uses only one MOSFET and one capacitor.

A dynamic RAM chip contains a large number of such logic cells.

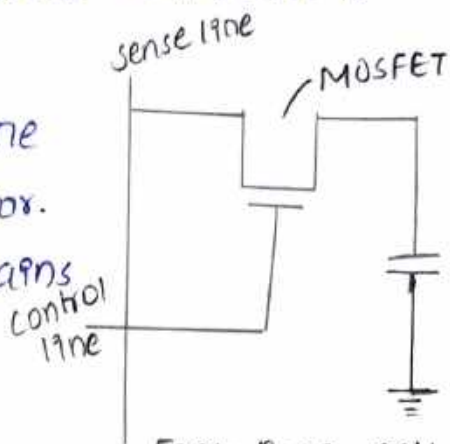


Fig:- Basic cell

When both the sense line and control line go high, the MOSFET conducts and the capacitor charges. When both lines go low, conduction ceases, since the MOSFET goes OFF. But the capacitor retains the charge. Thus a binary 1 is stored in the cell.

Advantage :-

- * Chip density is high

Disadvantage:-

The charge on the capacitor needs to be refreshed very frequently (after few milliseconds)

- * Requires Extra hardware & the system design is complex.